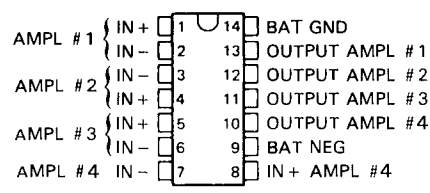
D2758, MARCH 1986–REVISED MARCH 1990

- Designed for −52-V Battery Operation
- 50-mA Output Current Capability
- Input Compatible with TTL and CMOS
- High Common-Mode Input Voltage Range
- Very Low Input Current
- Fail-Safe Disconnect Feature
- Built-In Output Clamp Diode
- Direct Replacement for National DS3680 and Fairchild μA3680

D OR N PACKAGE
(TOP VIEW)

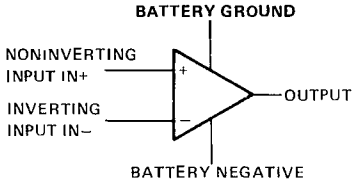


description

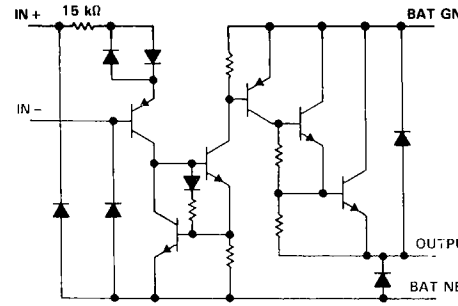
The DS3680I telephone relay driver is a monolithic integrated circuit designed to interface −48-V relay systems to TTL or other systems in telephone applications. It is capable of sourcing up to 50 mA from standard −52-V battery power. To reduce the effects of noise and IR drop between logic ground and battery ground, these drivers are designed to operate with a common-mode input range of ±20 V referenced to battery ground. The common-mode input voltages for the four drivers can be different, so a wide range of input elements can be accommodated. The high-impedance inputs are compatible with positive TTL and CMOS levels or negative logic levels. A clamp network is included in the driver outputs to limit high-voltage transients generated by the relay coil during switching. The complementary inputs ensure that the driver output will be "off" as a fail-safe condition when either output is open.

The DS3680I is characterized for operation from −40°C to 85°C.

symbol (each driver)



schematic diagram (each driver)



All resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range at BAT NEG, V_{B-} (see Note 1) . . . . . −70 V to 0.5 V
Input voltage range with respect to BAT GND . . . . . −70 V to 20 V
Input voltage range with respect to BAT NEG . . . . . −0.5 V to 70 V
Differential input voltage, V_{ID} (see Note 2) . . . . . ±20 V
Output current: resistive load . . . . . −100 mA
inductive load . . . . . −50 mA
Inductive output load . . . . . 5 H
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltages are with respect to the BAT GND terminal unless otherwise specified.
2. Differential input voltages are at the noninverting input terminal IN+ with respect to the inverting input terminal IN−.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW	494 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{B-}	−10	−60	V
Input voltage, either input	−20†	20	V
High-level differential input voltage, V_{IDH}	2	20	V
Low-level differential input voltage, V_{IDL}	−20†	0.8	V
Operating free-air temperature, T_A	−40	85	°C

†The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for input voltage levels.

electrical characteristics over recommended operating free-air temperature range, $V_{B-} = -52$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
I_{IH}	High-level input current (into IN+)	$V_{ID} = 2$ V			40	100	μA
		$V_{ID} = 7$ V			375	1000	
I_{IL}	Low-level input current (into IN+)	$V_{ID} = 0.4$ V			0.01	−5	μA
		$V_{ID} = -7$ V			−1	−3	
$V_{O(on)}$	On-state output voltage	$I_O = -50$ mA,	$V_{ID} = 2$ V		−1.6	−3	V
$I_{O(off)}$	Off-state output current	$V_O = V_{B-}$	$V_{ID} = 0.8$ V		−2	−100	μA
			Inputs open		−2	−100	
I_R	Clamp diode reverse current	$V_O = 0$			2	100	μA
V_{OK}	Output clamp voltage	$I_O = 50$ mA			0.9	1.2	V
		$I_O = -50$ mA,	$V_{B-} = 0$		−0.9	−1.2	
$I_{B(on)}$	On-state battery current	All drivers on			−2	−4.4	mA
$I_{B(off)}$	Off-state battery current	All drivers off			−1	−100	μA

‡All typical values are at $T_A = 25°C$.

switching characteristics V_{B-} = −52 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{on}	Turn-on time	V_{ID} = 3-V pulse,	R_L = 1 kΩ,		1	10	μs
t_{off}	Turn-off time	L = 1 H,	See Figure 2		1	10	μs

PARAMETER MEASUREMENT INFORMATION

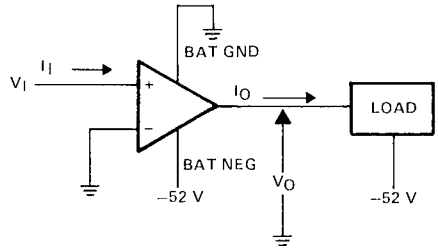


FIGURE 1. GENERALIZED TEST CIRCUIT, EACH DRIVER

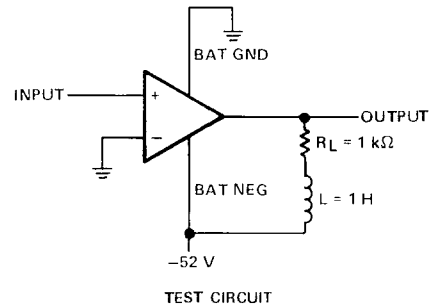


FIGURE 2. SWITCHING CHARACTERISTICS, EACH DRIVER

APPLICATION INFORMATION

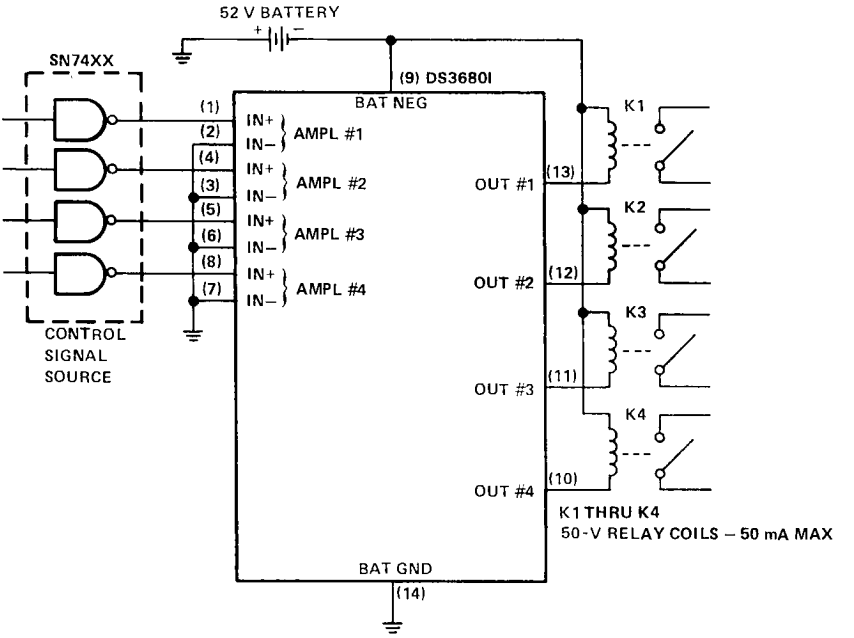
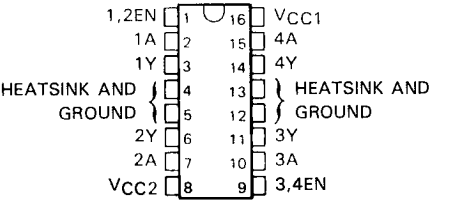


FIGURE 3. RELAY DRIVER

D2942, SEPTEMBER 1986—REVISED MAY 1990

- 1-A Output Current Capability Per Driver
- Pulsed Current 2-A Driver
- Wide Supply Voltage Range: 4.5 V to 36 V
- Separate Input-Logic Supply
- NE Package Designed for Heat Sinking
- Thermal Shutdown
- Internal ESD Protection
- High-Noise-Immunity Inputs
- Functional Replacement for SGS L293

NE PACKAGE
(TOP VIEW)



FUNCTION TABLE
(EACH DRIVER)

INPUTS†		OUTPUT
A	EN	Y
H	H	H
L	H	L
X	L	Z

H = high-level
L = low-level
X = irrelevant
Z = high-impedance (off)

†In the thermal shutdown mode, the output is in the high-impedance state regardless of the input levels.

description

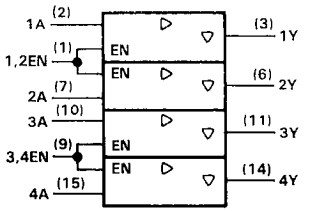
The L293 is a quadruple high-current half-H driver designed to provide bidirectional drive currents of up to one ampere at voltages from 4.5 V to 36 V. It is designed to drive inductive loads such as relays, solenoids, dc and bipolar stepping motors, as well as other high-current/high-voltage loads in positive-supply applications.

All inputs are TTL-compatible. Each output is a complete totem-pole drive circuit with a Darlington transistor sink and a psuedo-Darlington source. Drivers are enabled in pairs with drivers 1 and 2 enabled by 1,2EN and drivers 3 and 4 enabled by 3,4EN. When an enable input is high, the associated drivers are enabled and their outputs are active and in phase with their inputs. When the enable input is low, those drivers are disabled and their outputs are off and in a high-impedance state. With the proper data inputs, each pair of drivers form a full-H (or bridge) reversible drive suitable for solenoid or motor applications.

External high-speed output clamp diodes should be used for inductive transient suppression. A V_{CC1} terminal , separate from V_{CC2}, is provided for the logic inputs to minimize device power dissipation.

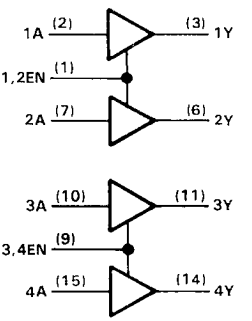
The L293 is designed for operation from 0°C to 70°C.

logic symbol‡

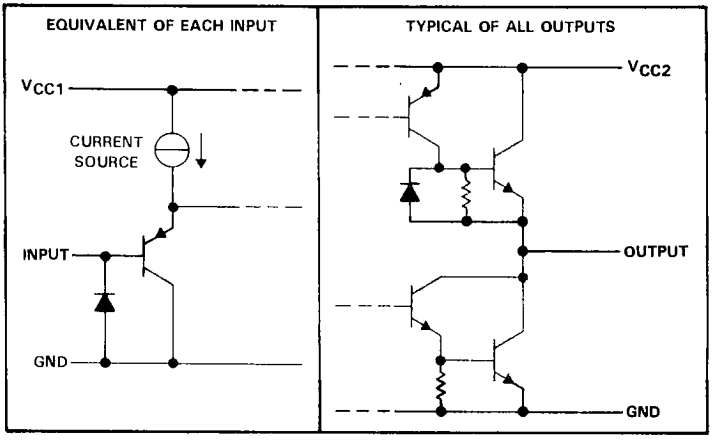


‡This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Logic supply voltage, V_{CC1} (see Note 1) . . . . . 36 V
Output supply voltage, V_{CC2} . . . . . 36 V
Input voltage . . . . . 7 V
Output voltage range . . . . . −3 V to V_{CC2}+3 V
Peak output current (nonrepetitive, t ≤ 5 ms) . . . . . ±2 A
Continuous output current . . . . . ±1 A
Continuous total dissipation at (or below) 25°C free-air temperature (see Notes 2 and 3) . . . . . 2075 mW
Continuous total dissipation at 80°C case temperature (see Note 3) . . . . . 5000 mW
Operating case or virtual junction temperature range . . . . . −40°C to 150°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 16.6 mW/°C.
3. For operation above 25°C case temperature, derate linearly at the rate of 71.4 mW/°C. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions

		MIN	MAX	UNIT
Logic supply voltage, V_{CC1}		4.5	7	V
Output supply voltage, V_{CC2}			36	V
High-level input voltage, V_{IH}	V_{CC1} ≤ 7 V	2.3		V
	V_{CC1} ≥ 7 V	2.3	7	
Low-level input voltage, V_{IL}		−0.3†	1.5	V
Operating free-air temperature, T_A		0	70	°C

†The algebraic convention, in which the least positive (most negative) designated minimum, is used in this data sheet for logic voltage levels.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

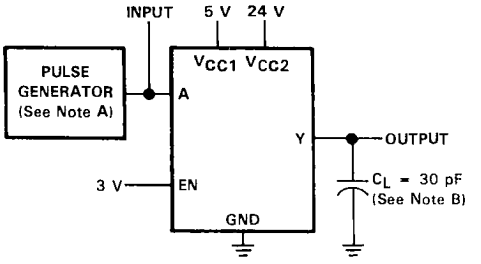
electrical characteristics, V_{CC1} = 5 V, V_{CC2} = 24 V, T_A = 25°C

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −1 A		V_{CC2}−1.8	V_{CC2}−1.4		V
V_{OL}	Low-level output voltage		I_{OL} = 1 A			1.2	1.8	V
I_{IH}	High-level input current	A	V_I = 7 V			0.2	100	μA
		EN				0.2	±10	
I_{IL}	Low-level input current	A	V_I = 0			−3	−10	μA
		EN				−2	−100	
I_{CC1}	Logic supply current		I_O = 0	All outputs at high level		13	22	mA
				All outputs at low level		35	60	
				All outputs at high impedance		8	24	
I_{CC2}	Output supply current		I_O = 0	All outputs at high level		14	24	mA
				All outputs at low level		2	6	
				All outputs at high impedance		2	4	

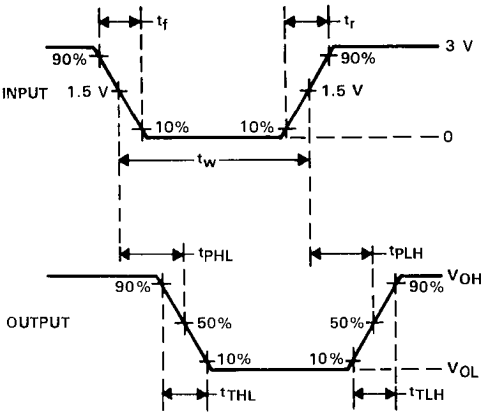
switching characteristics, V_{CC1} = 5 V, V_{CC2} = 24 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from A input	C_L = 30 pF, See Figure 1		800		ns
t_{PHL}	Propagation delay time, high-to-low-level output from A input			400		ns
t_{TLH}	Transition time, low-to-high-level output			300		ns
t_{THL}	Transition time, high-to-low-level output			300		ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, t_w = 10 μs, PRR = 5 kHz, Z_o = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING TIMES

APPLICATION INFORMATION

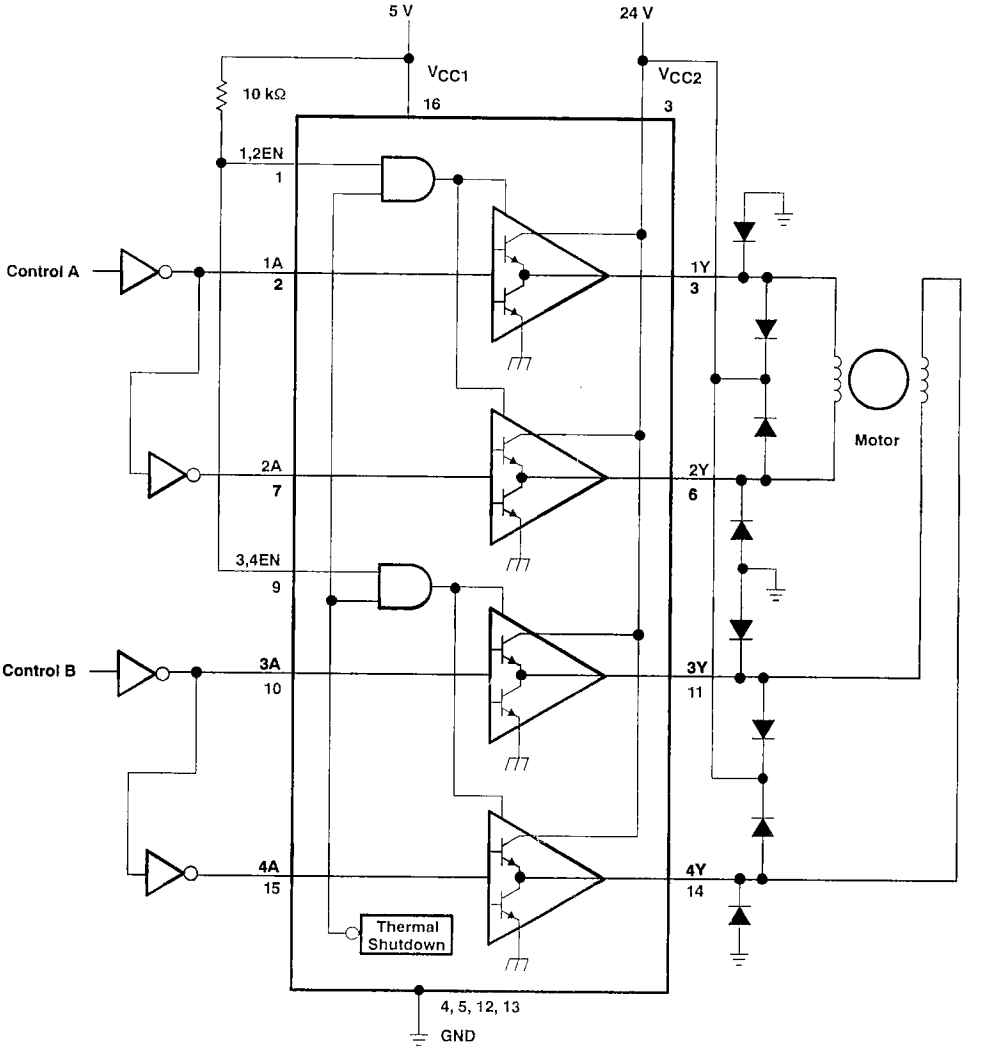


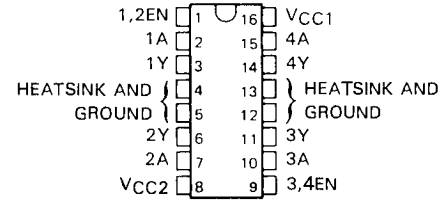
Figure 2. Two-Phase Motor Driver

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

D3511, SEPTEMBER 1986—REVISED MAY 1990

- 600-mA Output Current Capability Per Driver
- Pulsed Current 1.2-A Per Driver
- Output Clamp Diodes for Inductive Transient Suppression
- Wide Supply Voltage Range: 4.5 V to 36 V
- Separate Input-Logic Supply
- Thermal Shutdown
- Internal ESD Protection
- High-Noise-Immunity Inputs
- Functional Replacement for SGS L293D

NE PACKAGE
(TOP VIEW)



FUNCTION TABLE
(EACH DRIVER)

INPUTS†		OUTPUT
A	EN	Y
H	H	H
L	H	L
X	L	Z

H = high-level
L = low-level
X = irrelevant
Z = high-impedance (off)

†In the thermal shutdown mode, the output is in the high-impedance state regardless of the input levels.

description

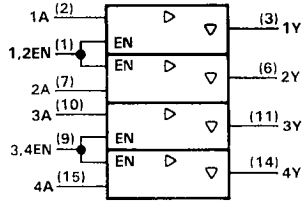
The L293D is a quadruple high-current half-H driver designed to provide bidirectional drive currents of up to 600 mA at voltages from 4.5 V to 36 V. It is designed to drive inductive loads such as relays, solenoids, dc and bipolar stepping motors, as well as other high-current/high-voltage loads in positive-supply applications.

All inputs are TTL-compatible. Each output is a complete totem-pole drive circuit with a Darlington transistor sink and a psuedo-Darlington source. Drivers are enabled in pairs with drivers 1 and 2 enabled by 1,2EN and drivers 3 and 4 enabled by 3,4EN. When an enable input is high,the associated drivers are enabled and their outputs are active and in phase with their inputs. When the enable input is low, those drivers are disabled and their outputs are off and in a high-impedance state. With the proper data inputs, each pair of drivers form a full-H (or bridge) reversible drive suitable for solenoid or motor applications.

A V_{CC1} terminal, separate from V_{CC2}, is provided for the logic inputs to minimize device power dissipation.

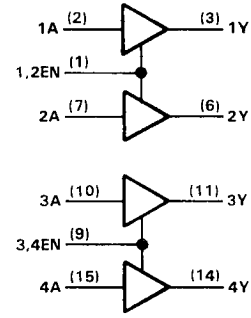
The L293D is designed for operation from 0°C to 70°C.

logic symbol‡

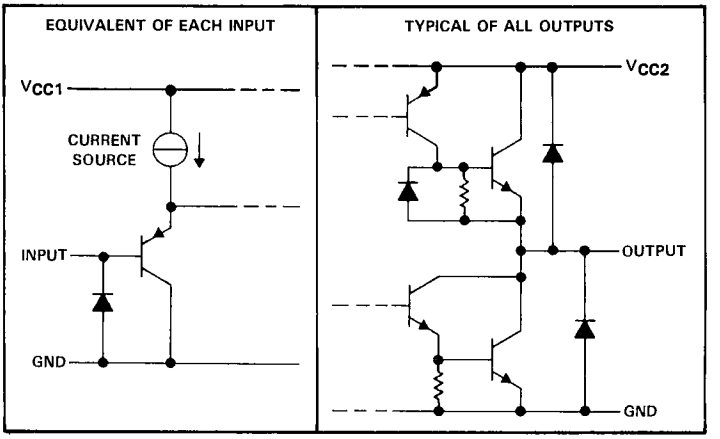


‡This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Logic supply voltage, V_{CC1} (see Note 1) . . . . . 36 V
Output supply voltage, V_{CC2} . . . . . 36 V
Input voltage . . . . . 7 V
Output voltage range . . . . . −3 V to V_{CC2} +3 V
Peak output current (nonrepetitive, t ≤ 100 μs) . . . . . ±1.2 A
Continuous output current . . . . . ±600 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Notes 2 and 3) . . . . . 2075 mW
Continuous total dissipation at 80°C case temperature (see Note 3) . . . . . 5000 mW
Operating case or virtual junction temperature range . . . . . −40°C to 150°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 16.6 mW/°C.
3. For operation above 25°C case temperature, derate linearly at the rate of 71.4 mW/°C. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions

		MIN	MAX	UNIT
Logic supply voltage, V_{CC1}		4.5	7	V
Output supply voltage, V_{CC2}		V_{CC1}	36	V
High-level input voltage, V_{IH}	$V_{CC1} \leq 7$ V	2.3	V_{CC1}	V
	$V_{CC1} \geq 7$ V	2.3	7	
Low-level input voltage, V_{IL}		−0.3†	1.5	V
Operating free-air temperature, T_A		0	70	°C

†The algebraic convention, in which the least positive (most negative) designated minimum, is used in this data sheet for logic voltage levels.

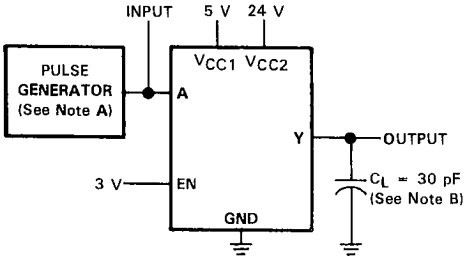
electrical characteristics, V_{CC1} = 5 V, V_{CC2} = 24 V, T_A = 25°C

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −0.6 A		V_{CC2}−1.8	V_{CC2}−1.4		V
V_{OL}	Low-level output voltage		I_{OL} = 0.6 A			1.2	1.8	V
V_{OKH}	High-level output clamp voltage		I_{OK} = 0.6 A			V_{CC2}+1.3		V
V_{OKL}	Low-level output clamp voltage		I_{OK} = −0.6 A			1.3		V
I_{IH}	High-level input current	A	V_I = 7 V			0.2	100	μA
		EN				0.2	±10	
I_{IL}	Low-level input current	A	V_I = 0			−3	−10	μA
		EN				−2	−100	
I_{CC1}	Logic supply current		I_O = 0	All outputs at high level		13	22	mA
				All outputs at low level		35	60	
				All outputs at high impedance		8	24	
I_{CC2}	Output supply current		I_O = 0	All outputs at high level		14	24	mA
				All outputs at low level		2	6	
				All outputs at high impedance		2	4	

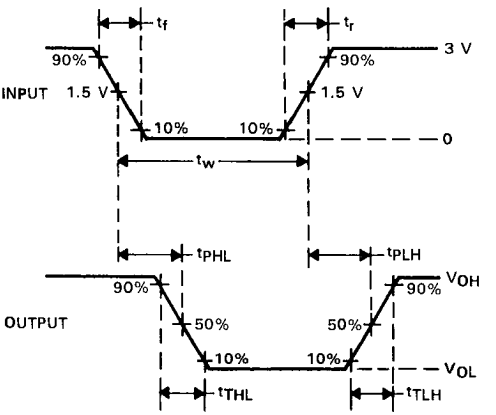
switching characteristics, V_{CC1} = 5 V, V_{CC2} = 24 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from A input	C_L = 30 pF, See Figure 1		800		ns
t_{PHL}	Propagation delay time, high-to-low-level output from A input			400		ns
t_{TLH}	Transition time, low-to-high-level output			300		ns
t_{THL}	Transition time, high-to-low-level output			300		ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, t_w = 10 μs, PRR = 5 kHz, Z_o = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING TIMES

APPLICATION INFORMATION

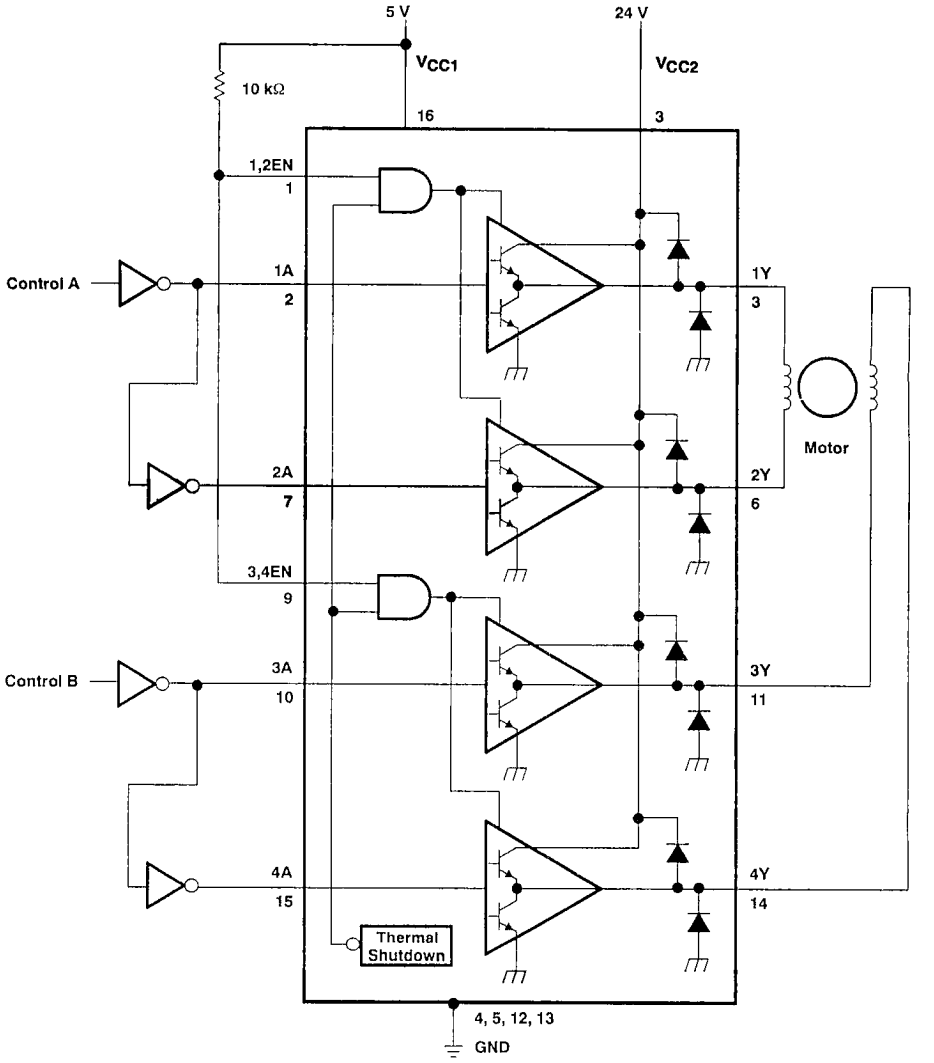


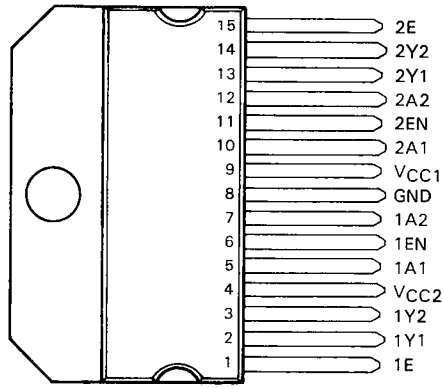
Figure 2. Two-Phase Motor Driver

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

D2942, OCTOBER 1986—REVISED JUNE 1990

- 2-A Output Current Capability per Full-H Driver
- Wide Range of Output Supply Voltage . . . 5 V to 46 V
- Separate Input-Logic Supply Voltage
- Thermal Shutdown
- Internal Electrostatic Discharge Protection
- High Noise Immunity
- Functional Replacement for SGS L298

KV PACKAGE
(TOP VIEW)



The tab is electrically connected to pin 8

description

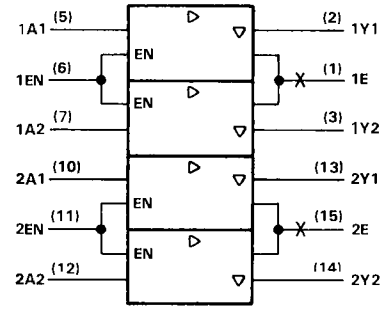
The L298 is a dual high-current full-H driver designed to provide bidirectional drive currents of up to two amperes at voltages from 5 V to 46 V. It is designed to drive inductive loads such as relays, solenoids, dc motors, stepping motors, and other high-current or high-voltage loads in positive-supply applications. All inputs are TTL compatible. Each output (Y) is a complete totem-pole drive with a Darlington transistor sink and a psuedo-Darlington source. Each full-H driver is enabled separately. Outputs 1Y1 and 1Y2 are enabled by 1EN and outputs 2Y1 and 2Y2 are enabled by 2EN. When an EN input is high, the associated channels are active. When an EN input is low, the associated channels are off (i.e., in the high-impedance state).

Each half of the device forms a full-H reversible driver suitable for solenoid or motor applications. The current in each full-H driver can be monitored by connecting a resistor between the sense output terminal 1E and ground and another resistor between sense output terminal 2E and ground.

External high-speed output-clamp diodes should be used for inductive transient suppression. To minimize device power dissipation, a V_{CC1} supply voltage, separate from V_{CC2}, is provided for the logic inputs.

The L298 is designed for operation from 0°C to 70°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

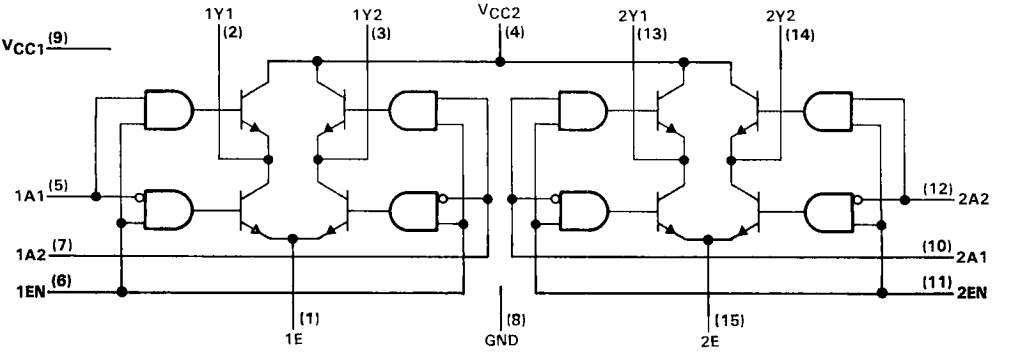
FUNCTION TABLE
(EACH CHANNEL)

INPUTS‡		OUTPUT
A	EN	Y
H	H	H
L	H	L
X	L	Z

‡ In the thermal shutdown mode, the outputs are in the high-impedance state regardless of the input levels.

H = high-level
L = low-level
X = irrelevant
Z = high-impedance (off)

logic diagram (positive logic)



absolute maximum ratings over operating temperature range (unless otherwise noted)

Logic supply voltage, V_{CC1}, (see Note 1) . . . . . 7 V
Output supply voltage, V_{CC2} . . . . . 50 V
Input voltage range at A or EN, V_I . . . . . −0.3 to 7 V
Output voltage range, V_O . . . . . −2 V to V_{CC2}+2 V
Emitter terminal (1E and 2E) voltage range . . . . . −0.5 to 2.3 V
Emitter terminal (1E and 2E) voltage (nonrepetitive, $t_w \leq 50\ \mu s$) . . . . . −1 V
Peak output current, I_{OM}, (nonrepetitive, $t_w \leq 0.1$ ms) . . . . . ±3 A
(repetitive, $t_w \leq 10$ ms, duty cycle ≤ 80%) . . . . . ±2.5 A
Continuous output current, I_O . . . . . ±2 A
Peak combined output current for each full-H driver (see Note 2)
(nonrepetitive, $t_w \leq 0.1$ ms) . . . . . ±3 A
(repetitive, $t_w \leq 10$ ms, duty cycle ≤ 80%) . . . . . ±2.5 A
Continuous combined output current for each full-H driver (see Note 2) . . . . . 3.575 W
Continuous dissipation at (or below) 25°C free-air temperature (see Note 3) . . . . . 3.575 W
Continuous dissipation at (or below) 75°C case temperature (see Note 3) . . . . . 25 W
Operating free-air, case, or virtual junction temperature range . . . . . −40°C to 150°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values are with respect to the network ground terminal, unless otherwise noted.
2. Combined output current applies to each of the two full-H drivers individually. This current is the sum of the currents at outputs 1Y1 and 1Y2 for full-H driver 1 and the sum of the currents at outputs 2Y1 and 2Y2 for full-H driver 2. The full-H drivers may carry the rated combined current simultaneously.
3. For operation above 25°C free-air temperature, derate linearly at the rate of 28.6 mW/°C. For operation above 75°C case temperature, derate linearly at the rate of 333 mW/°C. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions

		MIN	MAX	UNIT
Logic supply voltage, V_{CC1}		4.5	7	V
Output supply voltage, V_{CC2}		5	46	V
Emitter terminal (1E or 2E) voltage, V_E (see Note 4)		−0.5†	2	V
			$V_{CC1}-3.5$	
			$V_{CC2}-4$	
High-level input voltage, V_{IH} (see Note 4)	A	2.3	V_{CC1}	V
			$V_{CC2}-2.5$	
	EN	2.3	7	
			V_{CC1}	
Low-level input voltage at A or EN, V_{IL}		−0.3†	1.5	V
Output current, I_O			±2	A
Commutation frequency, f_c			40	kHz
Operating free-air temperature, T_A		0	70	°C

†The algebraic convention, in which the least positive (most negative) designated minimum, is used in this data sheet for emitter terminal voltage and logic voltage levels.

NOTE 4: For optimum device performance, the maximum recommended voltage at any A input is 2.5 V lower then V_{CC2}, the maximum recommended voltage at any EN input is V_{CC1}, and the maximum recommended voltage at any emitter terminal is 3.5 V lower than V_{CC1} and 4 V lower than V_{CC2}.

electrical characteristics, V_{CC1} = 5 V, V_{CC2} = 42 V, V_E = 0, T_J = 25°C (unless otherwise noted)

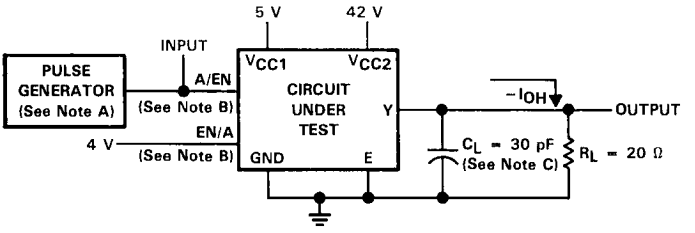
PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −1 A		$V_{CC2}-1.8$	$V_{CC2}-1.2$		V
			I_{OH} = −2 A		$V_{CC2}-2.8$	$V_{CC2}-1.8$		
V_{OL}	Low-level output voltage		I_{OL} = 1 A			$V_E+1.2$	$V_E+1.8$	V
			I_{OL} = 2 A			$V_E+1.7$	$V_E+2.6$	
V_{drop}	Total source plus sink output voltage drop		I_{OH} = −1 A, I_{OL} = 1 A	See Note 5		2.4	3.4	V
			I_{OH} = −2 A, I_{OL} = 2 A			3.5	5.2	
I_{IH}	High-level input current	A	$V_I = V_{IH}$			30	100	μA
		EN	$V_I = V_{IH} \le V_{CC1}-0.6$ V			30	100	
I_{IL}	Low-level input current		V_I = 0 to 1.5 V				−10	μA
I_{CC1}	Logic supply current		I_O = 0	All outputs at high level		7	12	mA
				All outputs at low level		24	32	
				All outputs at high impedance		4	6	
I_{CC2}	Output supply current		I_O = 0	All outputs at high level		38	50	mA
				All outputs at low level		13	20	
				All outputs at high impedance			2	

NOTE 5. The V_{drop} specification applies for I_{OH} and I_{OL} applied simultaneously to different output channels.
$V_{drop} = V_{CC2} - V_{OH} + V_{OL} - V_E$

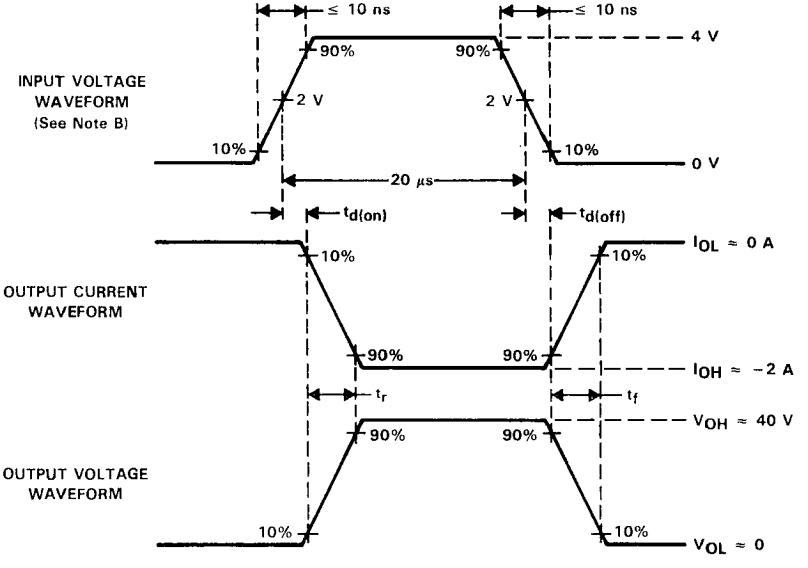
switching characteristics, V_{CC1} = 5 V, V_{CC2} = 42 V, V_E = 0, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Source current turn-on delay time from A input	C_L = 30 pF, See Figure 1		2.5		μs
$t_{d(off)}$	Source current turn-off delay time from A input			1.7		μs
t_r	Source current rise time (turning on)			0.4		μs
t_f	Source current fall time (turning off)			0.2		μs
$t_{d(on)}$	Source current turn-on delay time from EN input			2.5		μs
$t_{d(off)}$	Source current turn-off delay time from EN input			1.7		μs
$t_{d(on)}$	Sink current turn-on delay time from A input	C_L = 30 pF, See Figure 2		1.5		μs
$t_{d(off)}$	Sink current turn-off delay time from A input			0.7		μs
t_r	Sink current rise time (turning on)			0.2		μs
t_f	Sink current fall time (turning off)			0.2		μs
$t_{d(on)}$	Sink current turn-on delay time from EN input			1.5		μs
$t_{d(off)}$	Sink current turn-off delay time from EN input			0.7		μs

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

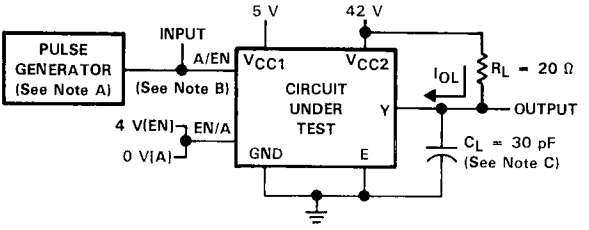


VOLTAGE AND CURRENT WAVEFORMS

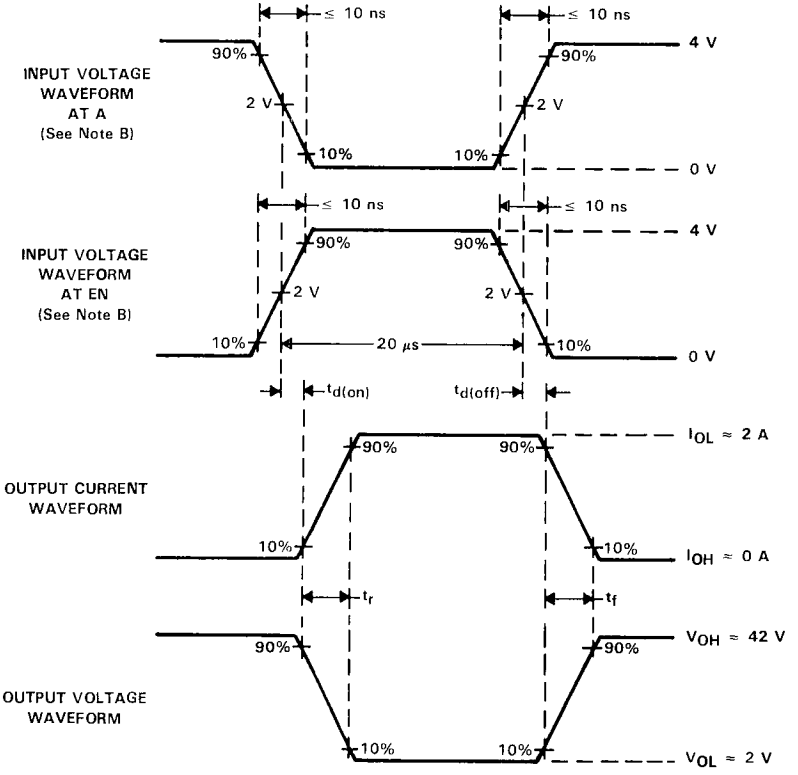
NOTES: A. The pulse generator has the following characteristics: PRR = 2 kHz, Z_O = 50 Ω.
B. EN is at 4 V if A is used as the switching input. A is at 4 V if EN is the switching input.
C. C_L includes probe and jig capacitance.

FIGURE 1. SOURCE CURRENT SWITCHING TIMES FROM DATA AND ENABLE INPUTS

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 2 kHz, Z_O = 50 Ω.
B. EN is at 4 V if A is used as the switching input. A is at 0 V if EN is the switching input.
C. C_L includes probe and jig capacitance.

FIGURE 2. SINK CURRENT SWITCHING TIMES FROM DATA AND ENABLE INPUTS

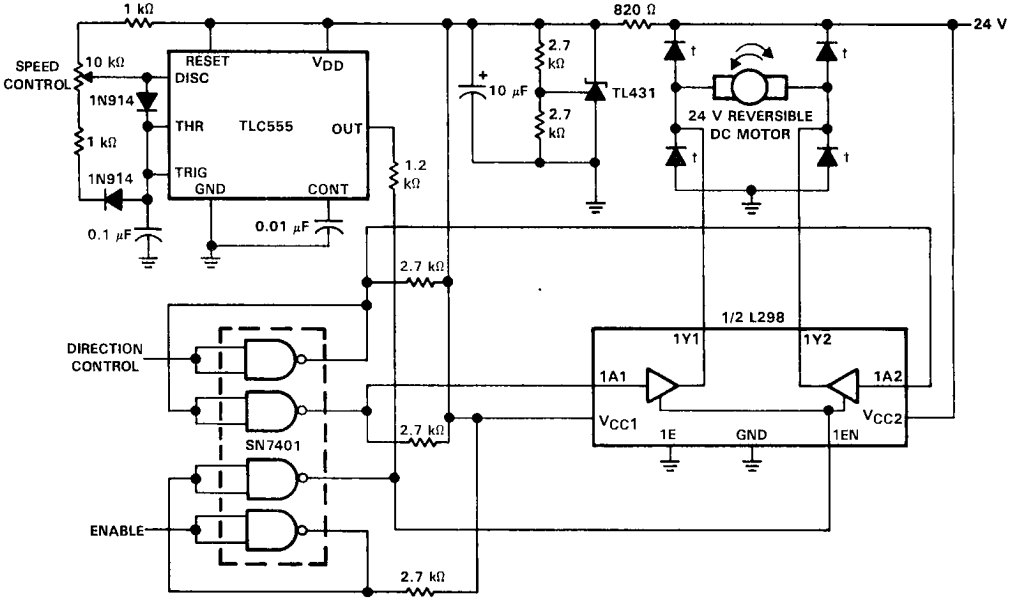
APPLICATION INFORMATION

This circuit shows one half of an L298 used to provide full-H bridge drive for a 24-V 2-A dc motor. Speed control is achieved with a TLC555 timer. This provides variable duty cycle pulses to the EN input of the L298. In this configuration, the operating frequency is approximately 1.2 kHz. The duty cycle is adjustable from 10% to 90% to provide a wide range of motor speeds. The motor direction is determined by the logic level at the direction control input. The circuit may be enabled or disabled by the logic level at the EN input. A 5-V supply for the logic and timer circuit is provided by a TL431 shunt regulator. For circuit operation, refer to the function table.

FUNCTION TABLE

ENABLE	DIRECTION CONTROL	1Y1	1Y2
H	H	source	sink
H	L	sink	source
L	**X**	**disabled**	**disabled**

X = don't care H = high level L = low level



†Diodes are 1N4934 or equivalent.

FIGURE 3. L298 AS BIDIRECTIONAL DC MOTOR DRIVER

PERIPHERAL DRIVERS FOR HIGH-CURRENT SWITCHING AT VERY HIGH SPEEDS

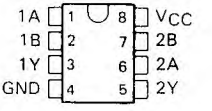
- Characterized for Use to 300 mA
- High-Voltage Outputs
- No Output Latch-Up at 20 V (After Conducting 300 mA)
- High-Speed Switching
- Circuit Flexibility for Varied Applications
- TTL-Compatible Diode-Clamped Inputs
- Standard Supply Voltages
- Plastic DIP (P) with Copper Lead Frame Provides Cooler Operation and Improved Reliability
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

SUMMARY OF SERIES 55451B/75451B

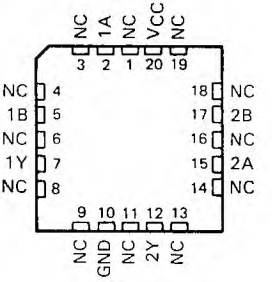
DEVICE	LOGIC OF COMPLETE CIRCUIT	PACKAGES
SN55451B	AND†	FK,JG
SN55452B	NAND	FK,JG
SN55453B	OR	FK,JG
SN55454B	NOR	FK,JG
SN75451B	AND	D,P
SN75452B	NAND	D,P
SN75453B	OR	D,P
SN75454B	NOR	D,P

†With output transistor base connected externally to output of gate.

SN55451B, SN55452B,
SN55453B, SN55454B . . . JG PACKAGE
SN75451B, SN75452B,
SN75453B, SN75454B . . . D OR P PACKAGE
(TOP VIEW)



SN55451B, SN55452B,
SN55453B, SN55454B, . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

Series SN55451B/75451B dual peripheral drivers are a family of versatile devices designed for use in systems that employ TTL logic. This family is functionally interchangeable with and replaces the SN75450 family and the SN75450A family devices manufactured previously. The speed of the SN55451B/SN75451B family is equal to that of the SN75450 family, and the parts are designed to ensure freedom from latch-up. Diode-clamped inputs simplify circuit design. Typical applications include high-speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers.

The SN55451B/SN75451B, SN55452B/SN75452B, SN55453B/SN75453B, and SN55454B/SN75454B are dual peripheral AND, NAND, OR, and NOR drivers, respectively, (assuming positive logic), with the output of the logic gates internally connected to the bases of the n-p-n output transistors.

Series SN55451B drivers are characterized for operation over the full military range of −55°C to 125°C. Series SN75451B drivers are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN55451B SN55452B SN55453B SN55454B	SN75451B SN75452B SN75453B SN75454B	UNIT
Supply voltage, V_{CC} (see Note 1)		7	7	V
Input voltage		5.5	5.5	V
Interemitter voltage (see Note 2)		5.5	5.5	V
Off-state output voltage		30	30	V
Continuous collector or output current (see Note 4)		400	400	mA
Peak collector or output current ($t_w \leq 10$ ms, duty cycle $\leq 50\%$, see Note 4)		500	500	mA
Continuous total power dissipation		See	ipation Rating Table	
Operating free-air temperature range, T_A		−55 to	0 to 70	°C
Storage temperature range		−65 to 150	−65 to 150	°C
Case temperature for 60 seconds	FK package			°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG package			°C
Lead temperature 1,6 mm (1,16 inch) from case for 10 seconds	D or P package		260	°C

NOTES: 1. Voltage values are with respect to the network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω.
4. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

DISSIPATION RATING TABLE

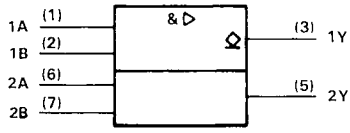
PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	—

recommended operating conditions

	SERIES 55451B			SERIES 75451B			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8			0.8	V
Operating free-air temperature, T_A	−55		125	0		70	°C

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

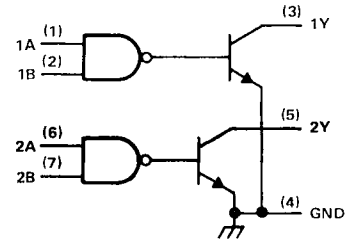
FUNCTION TABLE
(EACH DRIVER)

A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

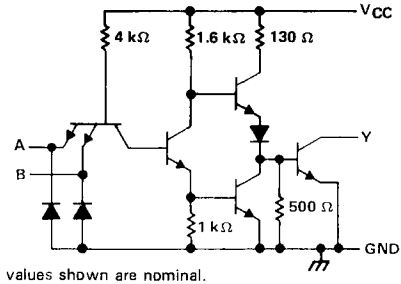
positive logic: $Y = AB$ or $\overline{\overline{A}+\overline{B}}$

Pin numbers shown are for D, JG, and P packages.

logic diagram (positive logic)



schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

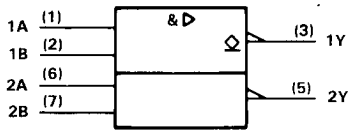
PARAMETER		TEST CONDITIONS‡	SN55451B MIN	SN55451B TYP§	SN55451B MAX	SN75451B MIN	SN75451B TYP§	SN75451B MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = MIN, V_{OH} = 30 V			300			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 5 V		7	11		7	11	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 0		52	65		52	65	mA

‡For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

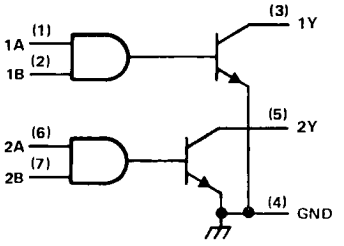
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 1		18	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output				18	25	ns
t_{TLH}	Transition time, low-to-high-level output				5	8	ns
t_{THL}	Transition time, high-to-low-level output				7	12	ns
V_{OH}	High-level output voltage after switching	SN55451B	V_S = 20 V, I_O ≈ 300 mA, See Figure 2		V_S−6.5		mV
		SN75451B			V_S−6.5		

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

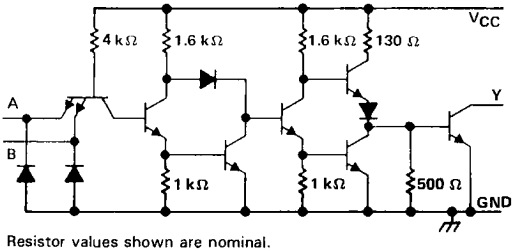


FUNCTION TABLE
(EACH DRIVER)

A	B	Y
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

positive logic
$Y = \overline{AB}$ or $\overline{A} + \overline{B}$

schematic (each driver)



Pin numbers shown are for D, JG, and P packages.

Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

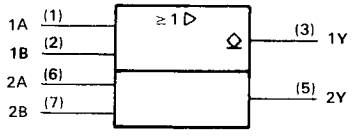
PARAMETER		TEST CONDITIONS‡		SN55452B			SN75452B			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{OH} = 30 V	V_{IL} = 0.8 V			300			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 100 mA	V_{IH} = MIN		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, I_{OL} = 300 mA	V_{IH} = MIN,		0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V		−1.1	−1.6		−1.1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX,	V_I = 0		11	14		11	14	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX,	V_I = 5 V		56	71		56	71	mA

‡For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 1		26	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output				24	35	ns
t_{TLH}	Transition time, low-to-high-level output				5	8	ns
t_{THL}	Transition time, high-to-low-level output				7	12	ns
V_{OH}	High-level output voltage after switching	SN55452B	V_S = 20 V, I_O ≈ 300 mA, See Figure 2	V_S−6.5			mV
		SN75452B		V_S−6.5			

logic symbol†



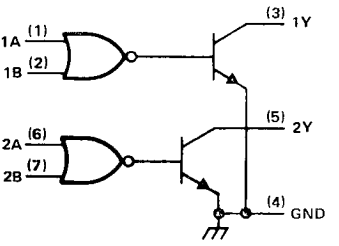
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE
(EACH DRIVER)

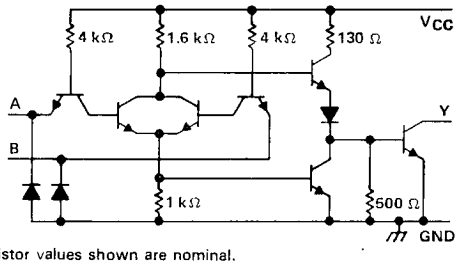
A	B	Y
L	L	L (on state)
L	H	H (off state)
H	L	H (off state)
H	H	H (off state)

positive logic
$Y = A + B$ or $\overline{\overline{A}\,\overline{B}}$

logic diagram (positive logic)



schematic (each driver)



Pin numbers shown are for D, JG, and P packages.

Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

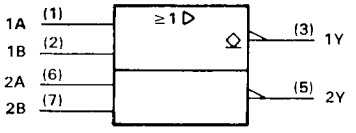
PARAMETER		TEST CONDITIONS‡		SN55453B			SN75453B			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{OH} = 30 V	V_{IH} = MIN,			300			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 100 mA	V_{IL} = 0.8 V,		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, I_{OL} = 300 mA	V_{IL} = 0.8 V,		0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX,	V_I = 5 V		8	11		8	11	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX,	V_I = 0		54	68		54	68	mA

‡For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 1		18	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output				16	25	ns
t_{TLH}	Transition time, low-to-high-level output				5	8	ns
t_{THL}	Transition time, high-to-low-level output				7	12	ns
V_{OH}	High-level output voltage after switching	SN55453B	V_S = 20 V, I_O ≈ 300 mA, See Figure 2		V_S−6.5		mV
		SN75			V_S−6.5		

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

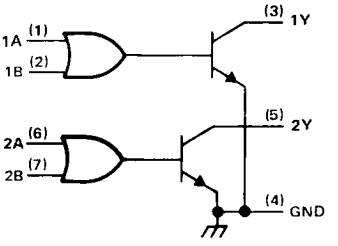
FUNCTION TABLE
(EACH DRIVER)

A	B	Y
L	L	H (off state)
L	H	L (on state)
H	L	L (on state)
H	H	L (on state)

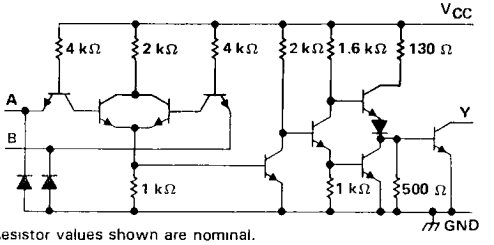
positive logic:
Y $\overline{A+B}$ or $\overline{AB}$

Pin numbers shown are for D, JG, and P packages.

logic diagram (positive logic)



schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

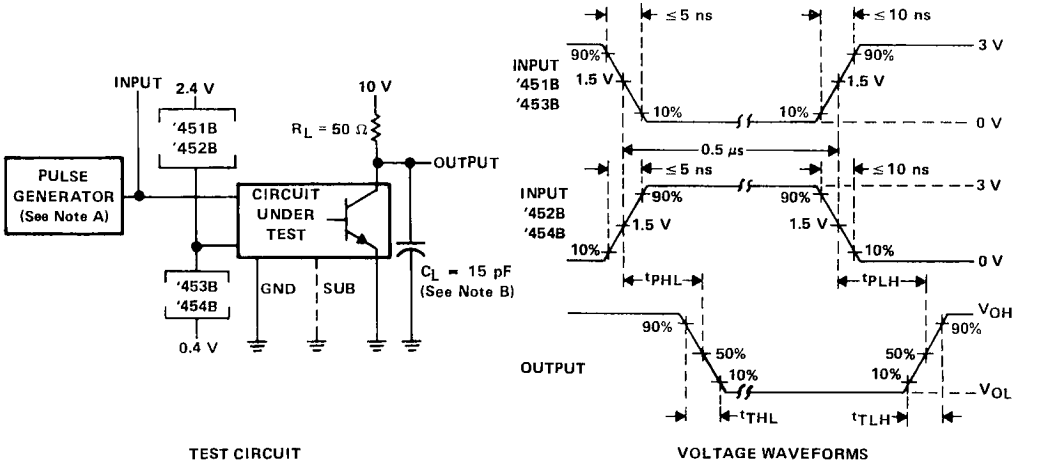
PARAMETER		TEST CONDITIONS‡		SN55454B			SN75454B			UNIT
				MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{OH} = 30 V	V_{IL} = 0.8 V			300			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 100 mA	V_{IH} = MIN		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, I_{OL} = 300 mA	V_{IH} = MIN,		0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX,	V_I = 0		13	17		13	17	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX,	V_I = 5 V		61	79		61	79	mA

‡For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

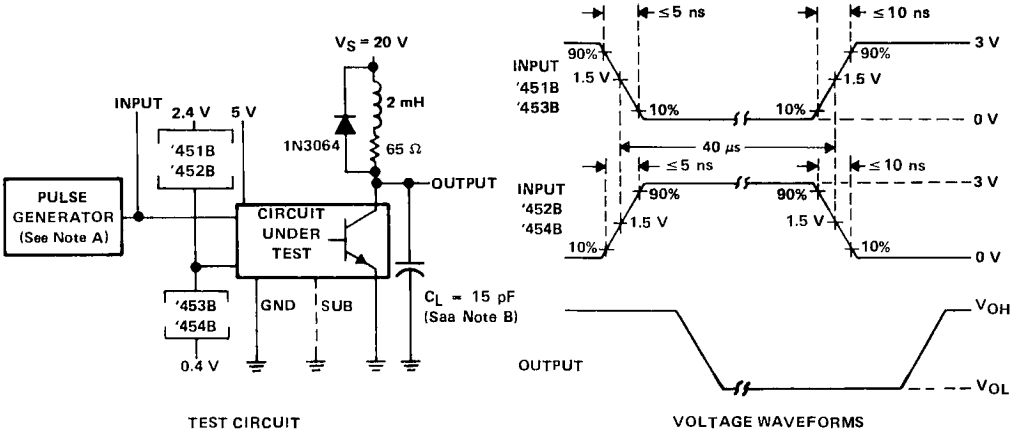
PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 1			27	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output					24	35	ns
t_{TLH}	Transition time, low-to-high-level output					5	8	ns
t_{THL}	Transition time, high-to-low-level output					7	12	ns
V_{OH}	High-level output voltage after switching	SN55454B	V_S = 20 V, I_O ≈ 300 mA, See Figure 2			V_S−6.5		mV
		'54B			V_S−6.5			

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, Z_O ≈ 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING TIMES OF COMPLETE DRIVERS

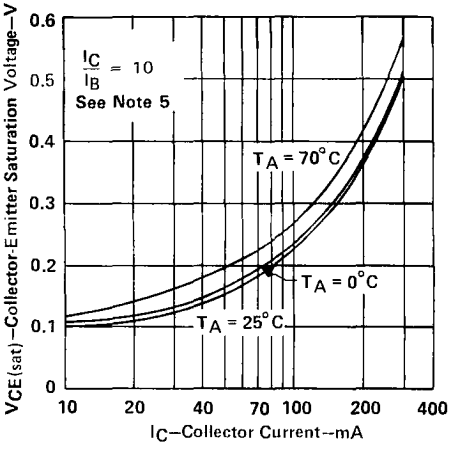


NOTES: A. The pulse generator has the following characteristics: PRR ≤ 12.5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 2. LATCH-UP TEST OF COMPLETE DRIVERS

TYPICAL CHARACTERISTICS

TRANSISTOR
COLLECTOR-EMITTER SATURATION VOLTAGE
vs
COLLECTOR CURRENT



NOTE 5: These parameters must be measured using pulse techniques, t_w = 300 μs, duty cycle ≤2%.

FIGURE 3

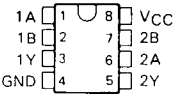
PERIPHERAL DRIVERS FOR HIGH-VOLTAGE, HIGH-CURRENT DRIVER APPLICATIONS

- Characterized for Use to 300 mA
- High-Voltage Outputs
- No Output Latch-Up at 30 V (After Conducting 300 mA)
- Medium-Speed Switching
- Circuit Flexibility for Varied Applications and Choice of Logic Function
- TTL-Compatible Diode-Clamped Inputs
- Standard Supply Voltages
- Plastic DIP (P) with Copper Lead Frame for Cooler Operation and Improved Reliability
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

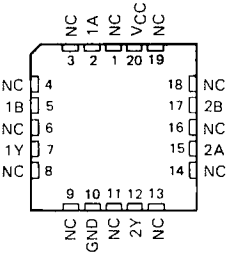
SUMMARY OF SERIES 55461/75461

[illegible]	LOGIC	PACKAGES
[illegible]	AND	FK,JG
[illegible] '62	NAND	FK,JG
[illegible] '63	OR	FK,JG
[illegible] '64	NOR	FK,JG
SN75461	AND	D,P
SN75462	NAND	D,P
SN75463	OR	D,P

SN55461, SN55462,
SN55463, SN55464 . . . JG PACKAGE
SN75461, SN75462,
SN75463 . . . D OR P PACKAGE
(TOP VIEW)



SN55461, SN55462,
SN55463, SN55464, . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

These dual peripheral drivers are functionally interchangeable with SN55451B through SN55454B and SN75451B through SN75453B peripheral drivers, but are designed for use in systems that require higher breakdown voltages than those devices can provide at the expense of slightly slower switching speeds. Typical applications include logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers.

The SN55461/SN75461, SN55462/SN75462, SN55463/SN75463, and SN55464 are dual peripheral AND, NAND, OR, and NOR drivers, respectively, (assuming positive logic), with the output of the gates internally connected to the bases of the n-p-n output transistors.

Series SN55461 drivers are characterized for operation over the full military temperature range of −55°C to 125°C; Series SN75461 drivers are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN55461 SN55462 SN55463 SN55464	SN75461 SN75462 SN75463	UNIT
Supply voltage, V_{CC} (see Note 1)		7	7	V
Input voltage		5.5	5.5	V
·emitter voltage (see Note 2)		5.5	5.5	V
Off-state output voltage		35	35	V
Continuous collector or output current (see Note 3)			400	mA
Peak collector or output current ($t_w \leq 10$ ms, duty cycle $\leq 50\%$, see Note 3)		500	500	mA
Continuous total power dissipation		See Dissipation Rating Table		
Operating free-air temperature range, T_A		−55 to	0 to 70	°C
Storage temperature range		−65 to	−65 to	°C
Case temperature for 60 seconds	FK package	260		°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG package	300		°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		260	°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

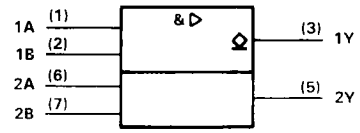
DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	—

recommended operating conditions

	SN55461 THRU SN55464			SN75461 THRU SN75463			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}			0.8				V
Operating free-air temperature, T_A	−55		125	0		70	°C

logic symbol†



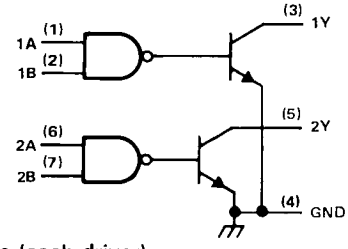
† This symbol is in accordance with ANSI/IEEE STD 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, JG, and P packages.

FUNCTION TABLE
(EACH DRIVER)

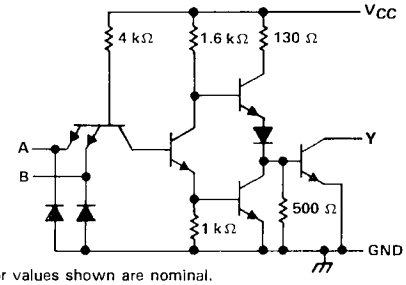
A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

positive logic:
$Y = AB$ or $\overline{\overline{A} + \overline{B}}$

logic diagram (positive logic)



schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

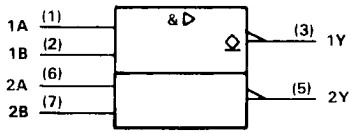
PARAMETER		TEST CONDITIONS†	SN55461 MIN	SN55461 TYP‡	SN55461 MAX	SN75461 MIN	SN75461 TYP‡	SN75461 MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = MIN, V_{OH} = 35 V			300			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 5 V		8	11		8	11	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 0		56	76		56	76	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditons.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

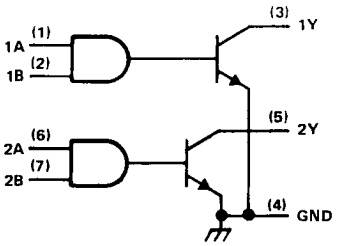
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 1		30	55	ns
t_{PHL}	Propagation delay time, high-to-low-level output			25	40	ns
t_{TLH}	Transition time, low-to-high-level output			8	20	ns
t_{THL}	Transition time, high-to-low-level output			10	20	ns
V_{OH}	High-level output voltage after switching SN55461	V_S = 30 V, I_O ≈ 300 mA, See Figure 2		V_S − 10		mV
	SN75461			V_S − 10		

logic symbol†



† This symbol is in accordance with ANSI/IEEE STD 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, JG, and P packages.

logic diagram (positive logic)

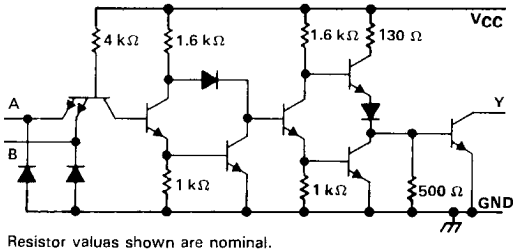


FUNCTION TABLE
(EACH DRIVER)

A	B	Y
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

positive logic:
$Y = \overline{AB}$ or $\overline{A} + \overline{B}$

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS†	SN55462 MIN	SN55462 TYP‡	SN55462 MAX	SN75462 MIN	SN75462 TYP‡	SN75462 MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V, V_{OH} = 35 V			300			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = MIN, I_{OL} = 100 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IH} = MIN, I_{OL} = 300 mA		0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1.1	−1.5		−1.1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 0		13	17		13	17	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 5 V		61	76		61	76	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 1		45	65	ns
t_{PHL}	Propagation delay time, high-to-low-level output			30	50	ns
t_{TLH}	Transition time, low-to-high-level output			13	25	ns
t_{THL}	Transition time, high-to-low-level output			10	20	ns
V_{OH}	High-level output voltage after switching	SN55462: V_S = 30 V, I_O ≈ 300 mA, See Figure 2		V_S−10		mV
		SN75462: V_S = 30 V, I_O ≈ 300 mA, See Figure 2		V_S−10		mV

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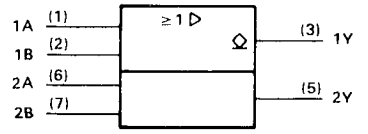
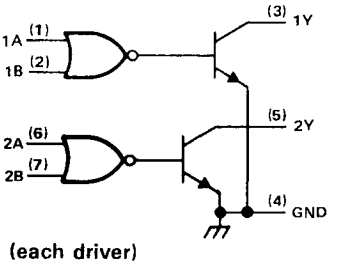
logic symbol†



†This symbol is in accordance with ANSI/IEEE STD 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, JG, and P packages.

logic diagram (positive logic)

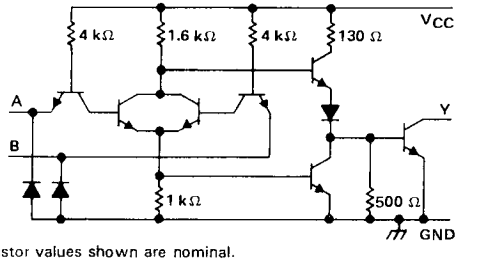


FUNCTION TABLE
(EACH DRIVER)

A	B	Y
L	L	L (on state)
L	H	H (off state)
H	L	H (off state)
H	H	H (off state)

positive logic:
$Y = A + B$ or $\overline{\overline{A}\,\overline{B}}$

schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

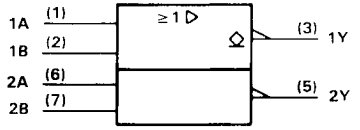
PARAMETER		TEST CONDITIONS†	SN55463			SN75463			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = MIN, V_{OH} = 35 V			300			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.5		0.25	0.4	V
		V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.8		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 5 V		8	11		8	11	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 0		58	76		58	76	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 1		30	55	ns
t_{PHL}	Propagation delay time, high-to-low-level output				25	40	ns
t_{TLH}	Transition time, low-to-high-level output				8	25	ns
t_{THL}	Transition time, high-to-low-level output				10	25	ns
V_{OH}	High-level output voltage after switching	SN55463	V_S = 30 V, I_O ≈ 300 mA, See Figure 2		V_S−10		mV
		SN75463		V_S−10			

logic symbol†



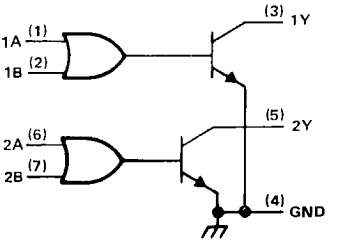
† This symbol is in accordance with ANSI/IEEE STD 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the JG package.

FUNCTION TABLE
(EACH DRIVER)

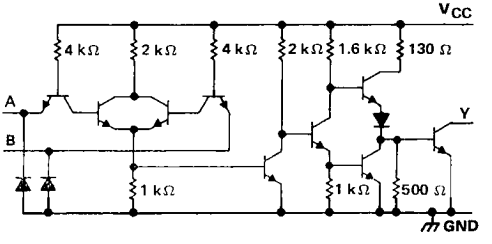
A	B	Y
L	L	H (off state)
L	H	L (on state)
H	L	L (on state)
H	H	L (on state)

positive logic:
$Y = \overline{A+B}$ or $\overline{A}\,\overline{B}$

logic diagram (positive logic)



schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

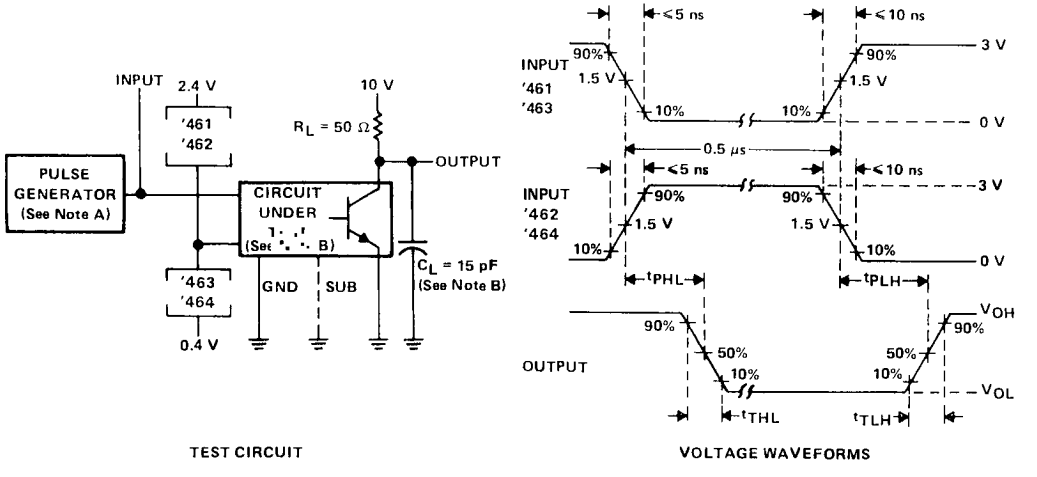
PARAMETER		TEST CONDITIONS†	SN55464 MIN	SN55464 TYP‡	SN55464 MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V, V_{OH} = 35 V			300	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = MIN, I_{OL} = 100 mA		0.25	0.5	V
		V_{CC} = MIN, V_{IH} = MIN, I_{OL} = 300 mA		0.5	0.8	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, V_I = 0		14	19	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, V_I = 5 V		67	85	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		I_O ≈ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 1		40	65	ns
t_{PHL}	Propagation delay time, high-to-low-level output				30	50	ns
t_{TLH}	Transition time, low-to-high-level output				8	20	ns
t_{THL}	Transition time, high-to-low-level output				10	20	ns
V_{OH}	High-level output voltage after switching	SN55464	V_S = 30 V, I_O ≈ 300 mA, See Figure 2	V_S−10			mV
		SN75464		V_S−10			

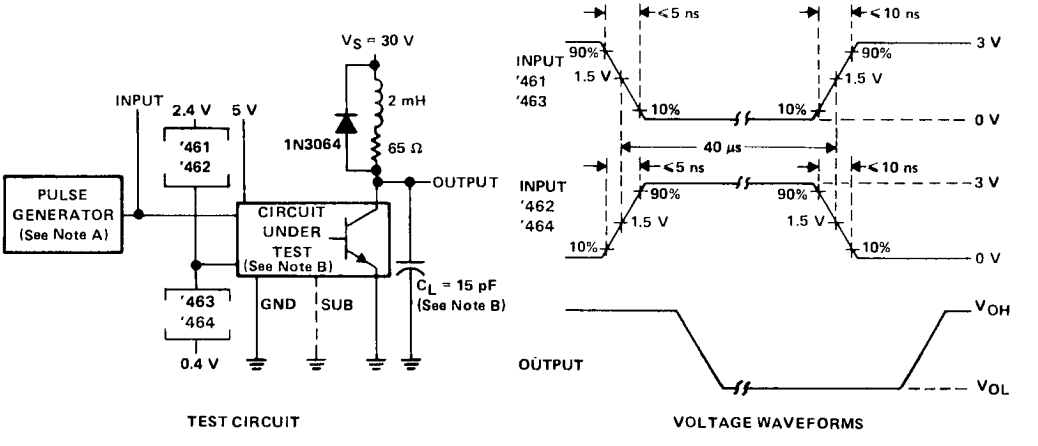
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHZ, Z_{out} ≈ 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING TIMES



TEST CIRCUIT VOLTAGE WAVEFORMS

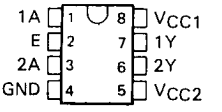
NOTES: A. The pulse generator has the following characteristics: PRR ≤ 12.5 kHz, Z_o = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 2. LATCH-UP TEST

D3004, JULY 1986

- Dual Circuits Capable of Driving High-Capacitance Loads at High Speeds
- Output Supply Voltage Range Up to 24 V
- Low Standby Power Dissipation

D OR P PACKAGE
(TOP VIEW)

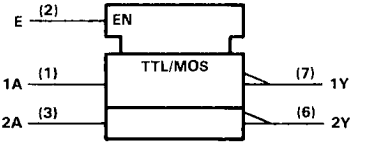


description

The SN75372 is a dual NAND gate interface circuit designed to drive power MOSFETs from TTL inputs. It provides high current and voltage levels necessary to drive large capacitive loads at high speeds. The device operates from a V_{CC1} of 5 V and a V_{CC2} of up to 24 V.

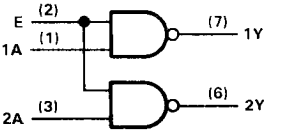
The SN75372 is characterized for operation from 0°C to 70°C.

logic symbol†

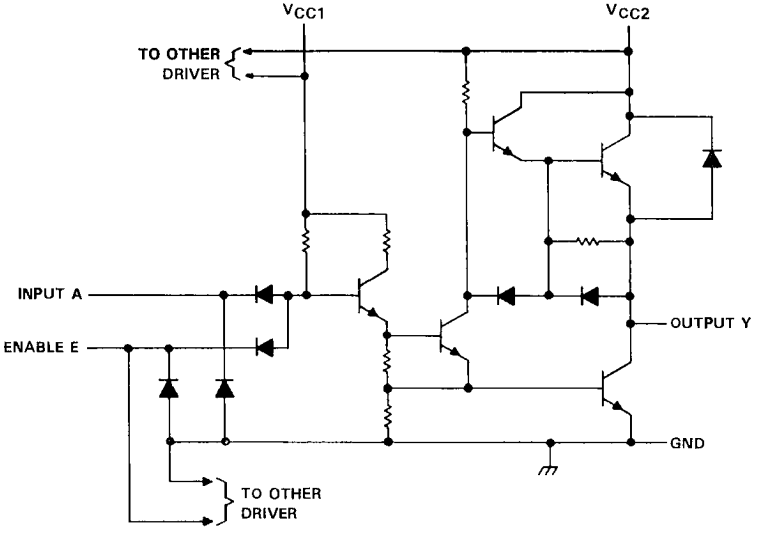


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic (each driver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC1} (see Note 1) . . . . . −0.5 V to 7 V
Supply voltage range of V_{CC2} . . . . . −0.5 V to 25 V
Input voltage . . . . . 5.5 V
Peak output current (t_w < 10 ms, duty cycle < 50%): Sink . . . . . 500 mA
Source . . . . . 500 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.75	5	5.25	V
Supply voltage, V_{CC2}	4.75	20	24	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−10	mA
Low-level output current, I_{OL}			40	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, and operating free-air temperature (unless otherwise noted)

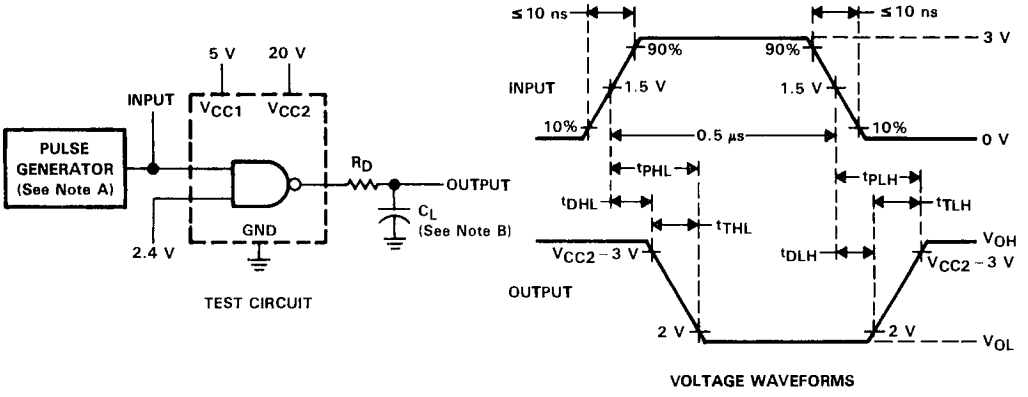
PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage		V_{IL} = 0.8 V,	I_{OH} = −50 μA	V_{CC2}−1.3	V_{CC2}−0.8		V
			V_{IL} = 0.8 V,	I_{OH} = −10 mA	V_{CC2}−2.5	V_{CC2}−1.8		
V_{OL}	Low-level output voltage		V_{IH} = 2 V,	I_{OL} = 10 mA		0.15	0.3	V
			V_{CC2} = 15 V to 24 V, I_{OL} = 40 mA	V_{IH} = 2 V,		0.25	0.5	
V_F	Output clamp diode forward voltage		V_I = 0,	I_F = 20 mA			1.5	V
I_I	Input current at maximum input voltage		V_I = 5.5 V				1	mA
I_{IH}	High-level input current	Any A	V_I = 2.4 V				40	μA
		Any E					80	
I_{IL}	Low-level input current	Any A	V_I = 0.4 V			−1	−1.6	mA
		Any E				−2	−3.2	
$I_{CC1(H)}$	Supply current from V_{CC1}, both outputs high		V_{CC1} = 5.25 V, All inputs at 0 V,	V_{CC2} = 24 V, No load		2	4	mA
$I_{CC2(H)}$	Supply current from V_{CC2}, both outputs high						0.5	mA
$I_{CC1(L)}$	Supply current from V_{CC1}, both outputs low		V_{CC1} = 5.25 V, All inputs at 5 V,	V_{CC2} = 24 V, No load		16	24	mA
$I_{CC2(L)}$	Supply current from V_{CC2}, both outputs low					7	13	mA
$I_{CC2(S)}$	Supply current from V_{CC2}, standby condition		V_{CC1} = 0, All inputs at 5 V,	V_{CC2} = 24 V, No load			0.5	mA

†All typical values are at V_{CC1} = 5 V, V_{CC2} = 20 V, and T_A = 25°C.

switching characteristics, V_{CC1} = 5 V, V_{CC2} = 20 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLH}	Delay time, low-to-high-level output	C_L = 390 pF, R_D = 10 Ω, See Figure 1		20	35	ns
t_{DHL}	Delay time, high-to-low-level output			10	20	ns
t_{TLH}	Transition time, low-to-high-level output			20	30	ns
t_{THL}	Transition time, high-to-low-level output			20	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output		10	40	65	ns
t_{PHL}	Propagation delay time, high-to-low-level output		10	30	50	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING TIMES, EACH DRIVER

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

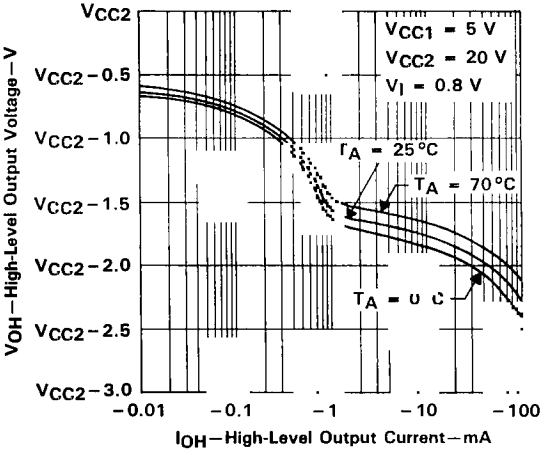


FIGURE 2

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

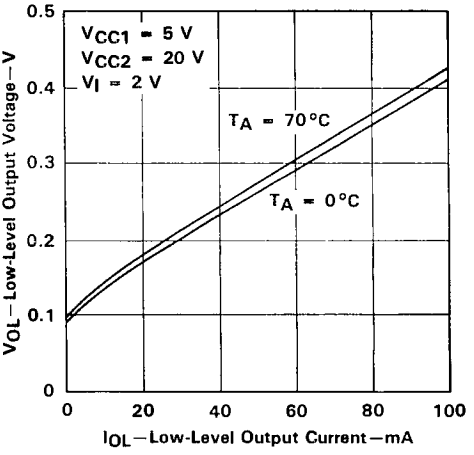


FIGURE 3

TYPICAL CHARACTERISTICS

VOLTAGE TRANSFER CHARACTERISTICS

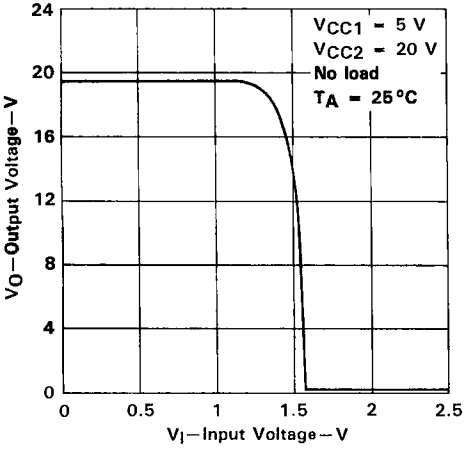


FIGURE 4

POWER DISSIPATION (BOTH DRIVERS)
vs
FREQUENCY

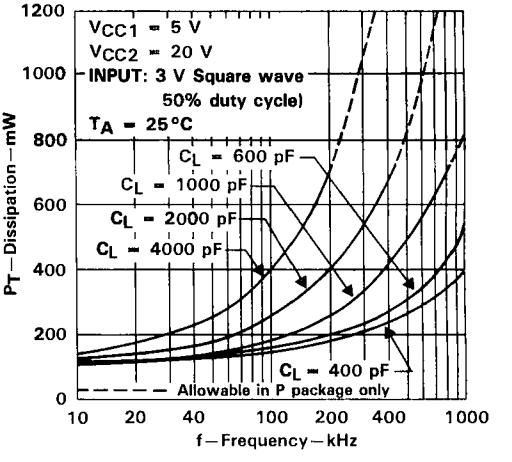


FIGURE 5

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

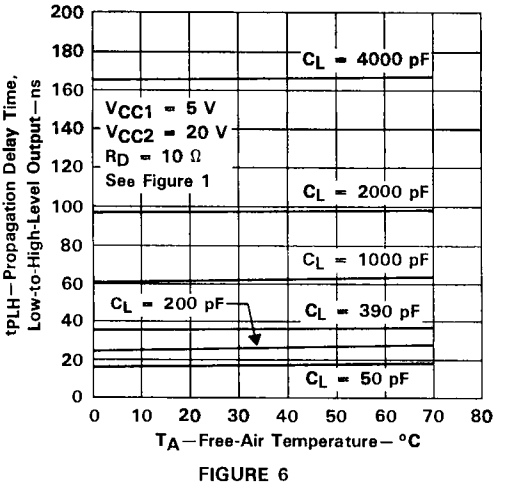


FIGURE 6

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

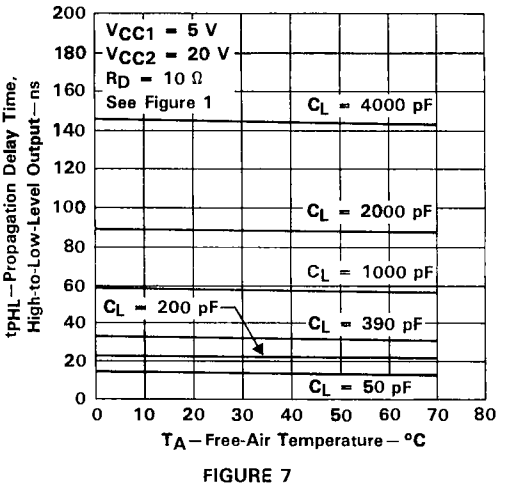


FIGURE 7

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
V_{CC2} SUPPLY VOLTAGE

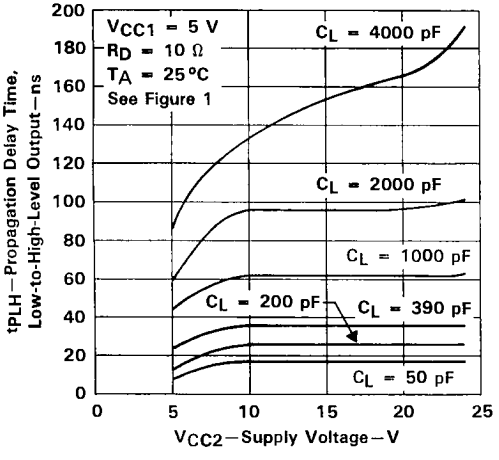


FIGURE 8

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
V_{CC2} SUPPLY VOLTAGE

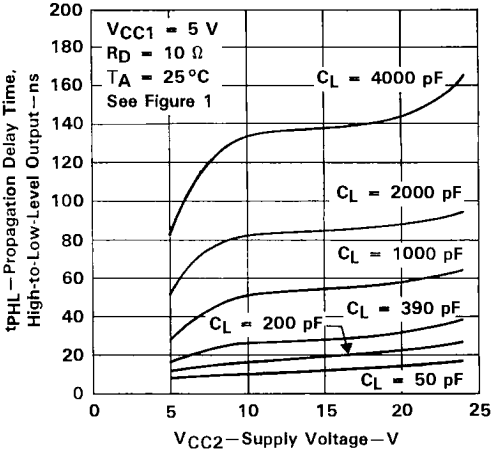


FIGURE 9

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
LOAD CAPACITANCE

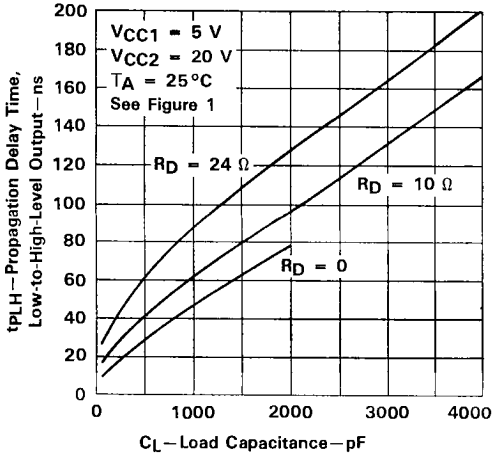


FIGURE 10

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
LOAD CAPACITANCE

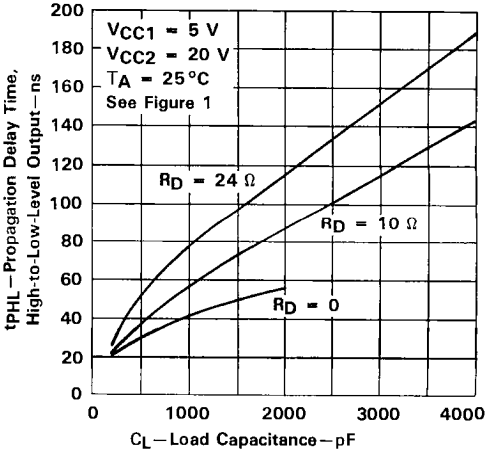


FIGURE 11

NOTE: For R_D = 0, operation with C_L > 2000 pF violates absolute maximum current rating.

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APPLICATIONS INFORMATION

driving power MOSFETs

The drive requirements of power MOSFETs are much lower than comparable bipolar power transistors. The input impedance of a FET consists of a reverse biased PN junction that can be described as a large capacitance in parallel with a very high resistance. For this reason, the commonly used open-collector driver with a pull-up resistor is not satisfactory for high-speed applications. In Figure 12(a), an IRF151 power MOSFET switching an inductive load is driven by an open-collector transistor driver with a 470-Ω pull-up resistor. The input capacitance (C_{iss}) specification for an IRF151 is 4000 pF maximum. The resulting long turn-on time due to the combination of C_{iss} and the pull-up resistor is shown in Figure 12(b).

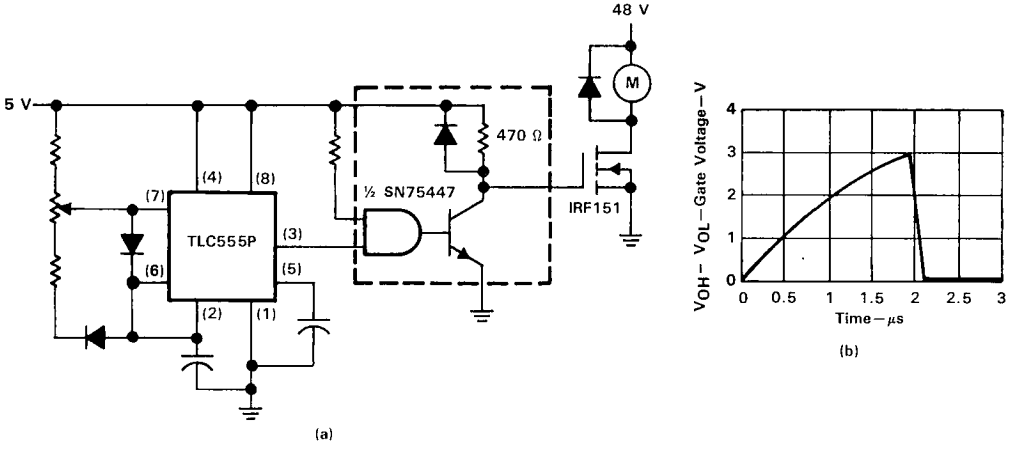


FIGURE 12. POWER MOSFET DRIVE USING SN75447

APPLICATIONS INFORMATION

A faster, more efficient drive circuit uses an active pull-up as well as an active pull-down output configuration, referred to as a totem-pole output. The SN75372 driver provides the high speed, totem-pole drive desired in an application of this type, see Figure 13(a). The resulting faster switching speeds are shown in Figure 13(b).

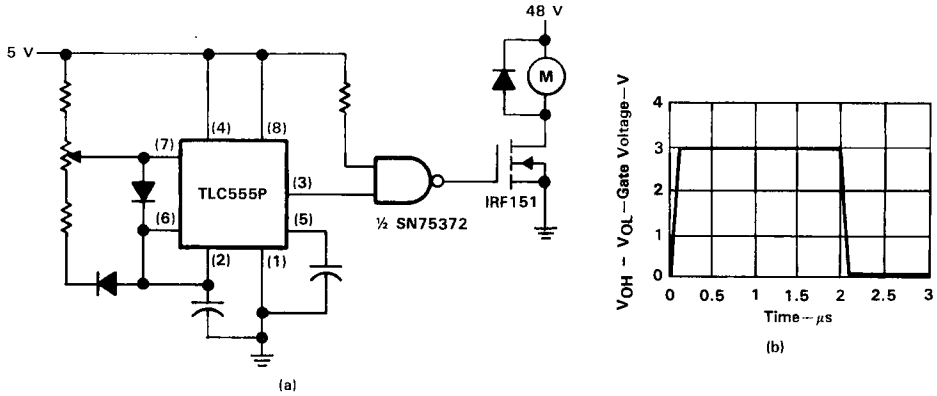


FIGURE 13. POWER MOSFET DRIVE USING SN75372

Power MOSFET drivers must be capable of supplying high peak currents to achieve fast switching speeds as shown by the equation

$$I_{pk} = \frac{VC}{t_r}$$

where C is the capacitive load, and t_r is the desired rise time. V is the voltage that the capacitance is charged to. In the circuit shown in Figure 13(a), V is found by the equation

$$V = V_{OH} - V_{OL}$$

Peak current required to maintain a rise time of 100 ns in the circuit of Figure 13(a) is

$$I_{PK} = \frac{(3\text{-}0)4(10^{-9})}{100(10^{-9})} = 120 \text{ mA}$$

Circuit capacitance can be ignored because it is very small compared to the input capacitance of the IRF151. With a V_{CC} of 5 V, and assuming worst-cast conditions, the gate drive voltage is 3 V.

For applications in which the full voltage of V_{CC2} must be supplied to the MOSFET gate, the SN75374 QUAD MOSFET driver should be used.

THERMAL INFORMATION

power dissipation precautions

Significant power may be dissipated in the SN75372 driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. Figure 5 shows the power dissipated in a typical SN75372 as a function of load capacitance and frequency. Average power dissipated by this driver is derived from the equation

$$P_{T(AV)} = P_{DC(AV)} + P_{C(AV)} + P_{S(AV)}$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load and all are averaged over a full cycle.

The power components per driver channel are

$$P_{DC(AV)} = \frac{P_H t_H + P_L t_L}{T}$$

$$P_{C(AV)} \approx C V_C^2 \quad f$$

$$P_{S(AV)} = \frac{P_{LH} t_{LH} + P_{HL} t_{HL}}{T}$$

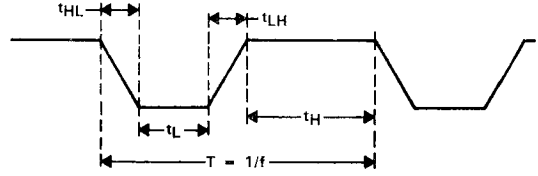


FIGURE 14. OUTPUT VOLTAGE WAVEFORM

where the times are as defined in Figure 14.

P_L, P_H, P_{LH}, and P_{HL} are the respective instantaneous levels of power dissipation, C is the load capacitance. V_C is the voltage across the load capacitance during the charge cycle shown by the equation

$$V_C = V_{OH} - V_{OL}$$

$P_{S(AV)}$ may be ignored for power calculations at low frequencies.

THERMAL INFORMATION

In the following power calculation, both channels are operating under identical conditions: V_{OH} = 19.2 V and V_{OL} = 0.15 V with V_{CC1} = 5 V, V_{CC2} = 20 V, V_C = 19.05 V, C = 1000 pF, and the duty cycle = 60%. At 0.5 MHz, $P_{S(AV)}$ is negligible and can be ignored. When the output voltage is high, I_{CC2} is negligible and can be ignored.

On a per-channel basis using data sheet values

$$P_{DC(AV)} = \left[(5\text{ V})\left(\frac{2\text{ mA}}{2}\right) + (20\text{ V})\left(\frac{0\text{ mA}}{2}\right)\right](0.6) + \left[(5\text{ V})\left(\frac{16\text{ mA}}{2}\right) + (20\text{ V})\left(\frac{7\text{ mA}}{2}\right)\right](0.4)$$

$P_{DC(AV}$ = 47 mW per channel

Power during the charging time of the load capacitance is

$P_{C(AV)}$ = (1000 pF) (19.05 V)^2 (0.5 MHz) = 182 mW per channel

Total power for each driver is

$P_{T(AV)}$ = 47 mW + 182 mW = 229 mW

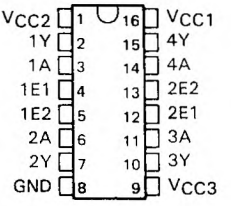
and total package power is

$P_{T(AV)}$ = (229) (2) = 458 mW.

D3004, SEPTEMBER 1986

- **Quadruple Circuits Capable of Driving High-Capacitance Loads at High Speeds**
- **Output Supply Voltage Range from 5 V to 24 V**
- **Low Standby Power Dissipation**
- **V_{CC3} Supply Maximizes Output Source Voltage**

D OR N PACKAGE
(TOP VIEW)



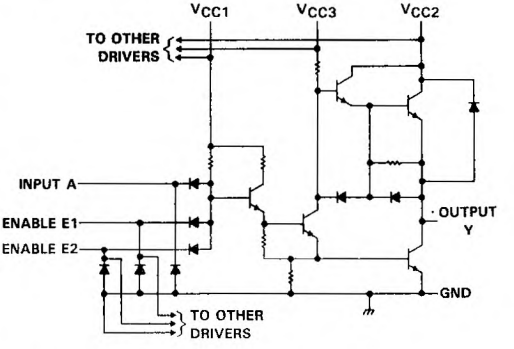
description

The SN75374 is a quadruple NAND interface circuit designed to drive power MOSFETs from TTL inputs. It provides the high current and voltage necessary to drive large capacitive loads at high speeds.

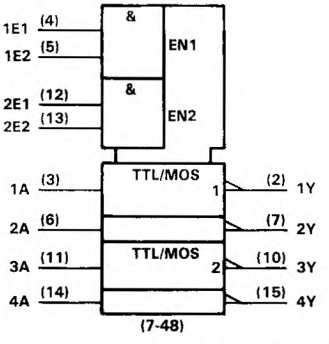
The outputs can be switched very close to the V_{CC2} supply rail when V_{CC3} is about 3 V higher than V_{CC2}. The V_{CC3} pin can also be tied directly to V_{CC2} when the source voltage requirements are lower.

The SN75374 is characterized for operation from 0°C to 70°C.

schematic (each driver)

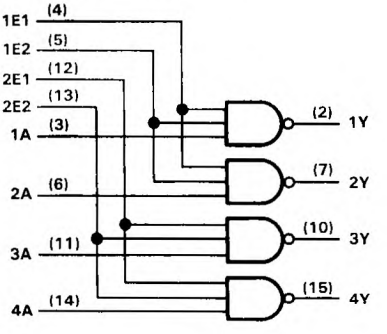


logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC1}, (see Note 1) . . . . . −0.5 V to 7 V
Supply voltage range of V_{CC2} . . . . . −0.5 V to 25 V
Supply voltage range of V_{CC3} . . . . . −0.5 V to 30 V
Input voltage . . . . . 5.5 V
Peak output current (t_w < 10 ms, duty cycle < 50%): Sink . . . . . 500 mA
Source . . . . . 500 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	4.75	5	5.25	V
Supply voltage, V_{CC2}	4.75	20	24	V
Supply voltage, V_{CC3}	V_{CC2}	24	28	V
Voltage difference between supply voltages: $V_{CC3} - V_{CC2}$	0	4	10	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−10	mA
Low-level output current, I_{OL}			40	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, V_{CC3}, and operating free-air temperature (unless otherwise noted)

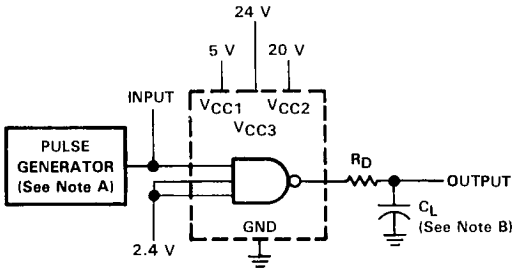
PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC3} = V_{CC2}+3 V,	V_{IL} = 0.8 V, I_{OH} = −100 μA	V_{CC2}−0.3	V_{CC2}−0.1		V
			V_{CC3} = V_{CC2}+3 V,	V_{IL} = 0.8 V, I_{OH} = −10 mA	V_{CC2}−1.3	V_{CC2}−0.9		
			V_{CC3} = V_{CC2},	V_{IL} = 0.8 V, I_{OH} = −50 μA	V_{CC2}−1	V_{CC2}−0.7		
			V_{CC3} = V_{CC2},	V_{IL} = 0.8 V, I_{OH} = −10 mA	V_{CC2}−2.5	V_{CC2}−1.8		
V_{OL}	Low-level output voltage		V_{IH} = 2 V,	I_{OL} = 10 mA		0.15	0.3	V
			V_{CC2} = 15 V to 28 V,	V_{IH} = 2 V, I_{OL} = 40 mA		0.25	0.5	
V_F	Output clamp diode forward voltage		V_I = 0,	I_F = 20 mA			1.5	V
I_I	Input current at maximum input voltage		V_I = 5.5 V				1	mA
I_{IH}	High-level input current	Any A	V_I = 2.4 V				40	μA
		Any E					80	
I_{IL}	Low-level input current	Any A	V_I = 0.4 V			−1	−1.6	mA
		Any E				−2	−3.2	
$I_{CC1(H)}$	Supply current from V_{CC1}, all outputs high		V_{CC1} = 5.25 V, V_{CC3} = 28 V, No load	V_{CC2} = 24 V, All inputs at 0 V,		4	8	mA
$I_{CC2(H)}$	Supply current from V_{CC2}, all outputs high					−2.2	0.25	
$I_{CC3(H)}$	Supply current from V_{CC3}, all outputs high					2.2	3.5	
$I_{CC1(L)}$	Supply current from V_{CC1}, all outputs low		V_{CC1} = 5.25 V, V_{CC3} = 28 V, No load	V_{CC2} = 24 V, All inputs at 5 V,		31	47	mA
$I_{CC2(L)}$	Supply current from [illegible] all outputs low						2	
$I_{CC3(L)}$	[illegible] current from V_{CC3}, all outputs low					16	27	
$I_{CC2(H)}$	Supply current from V_{CC2}, all outputs high		V_{CC1} = 5.25 V, V_{CC3} = 24 V, No load	V_{CC2} = 24 V, All inputs at 0 V,			0.25	mA
$I_{CC3(H)}$	Supply current from V_{CC3}, all outputs high						0.5	
$I_{CC2(S)}$	Supply current from V_{CC2}, standby condition		V_{CC1} = 0, V_{CC3} = 24 V, No load	V_{CC2} = 24 V, All inputs at 0 V,			0.25	mA
$I_{CC3(S)}$	Supply current from V_{CC3}, standby condition						0.5	

†All typical values are at V_{CC1} = 5 V, V_{CC2} = 20 V, V_{CC3} = 24 V, and T_A = 25°C except for V_{OH} for which V_{CC2} and V_{CC3} are as stated under test conditions.

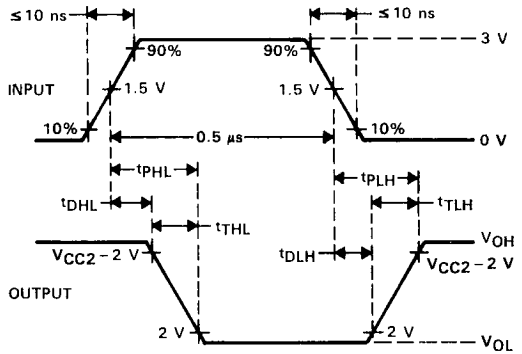
switching characteristics, V_{CC1} = 5 V, V_{CC2} = 20 V, V_{CC3} = 24 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLH}	Delay time, low-to-high-level output	C_L = 200 pF, R_D = 24 Ω, See Figure 1		20	30	ns
t_{DHL}	Delay time, high-to-low-level output			10	20	ns
t_{TLH}	Transition time, low-to-high-level output			20	30	ns
t_{THL}	Transition time, high-to-low-level output			20	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output		10	40	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output		10	30	50	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING TIMES, EACH DRIVER

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

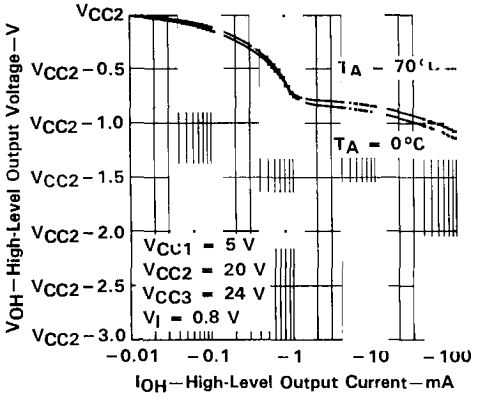


FIGURE 2

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

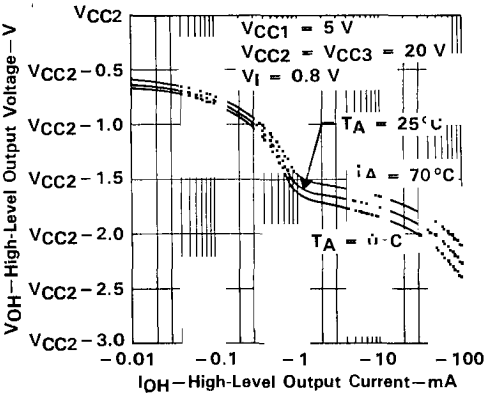


FIGURE 3

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

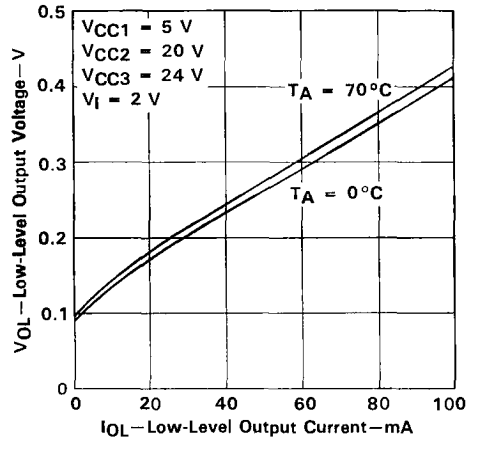


FIGURE 4

VOLTAGE TRANSFER CHARACTERISTICS

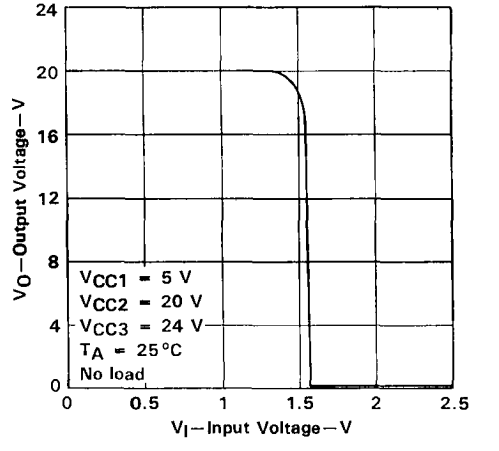


FIGURE 5

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

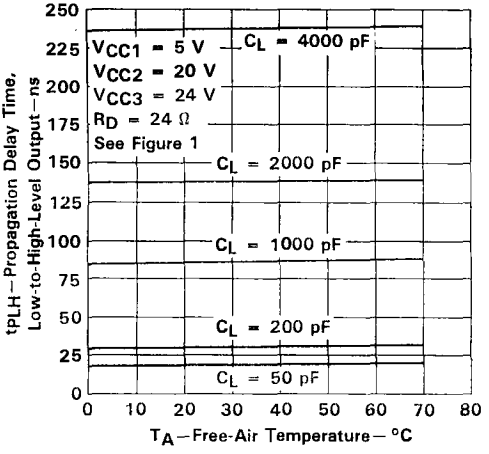


FIGURE 6

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
T_A-FREE-AIR TEMPERATURE

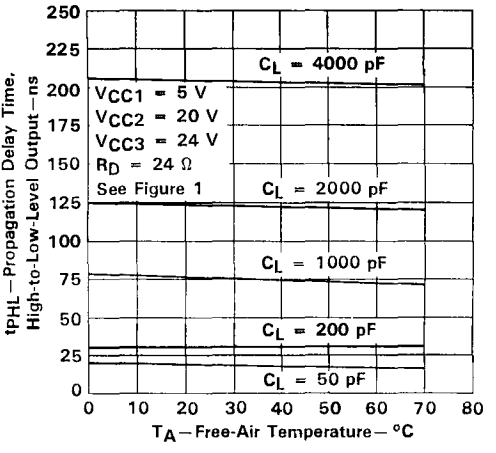


FIGURE 7

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
V_{CC2} SUPPLY VOLTAGE

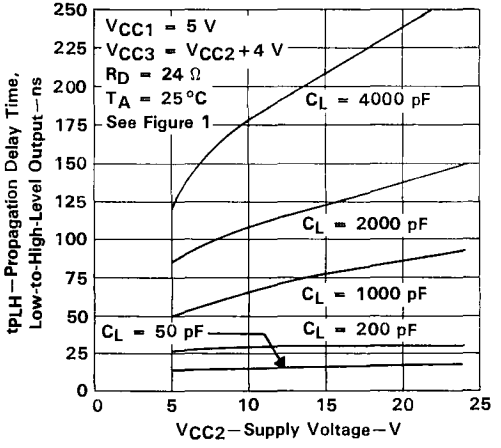


FIGURE 8

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
V_{CC2} SUPPLY VOLTAGE

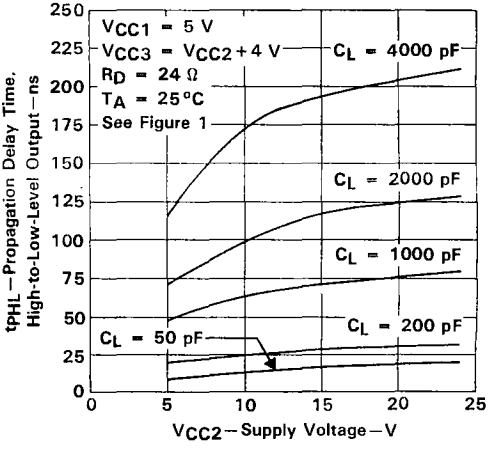


FIGURE 9

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
LOAD CAPACITANCE

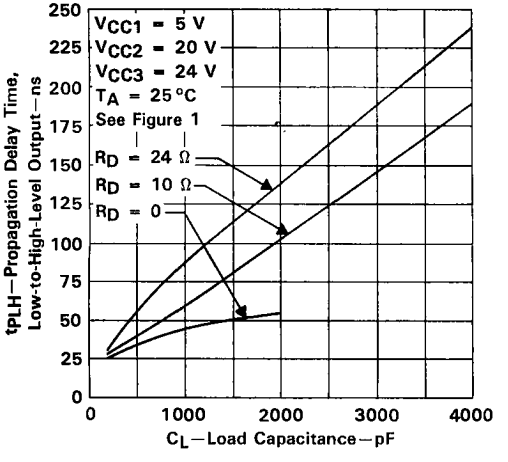


FIGURE 10

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
LOAD CAPACITANCE

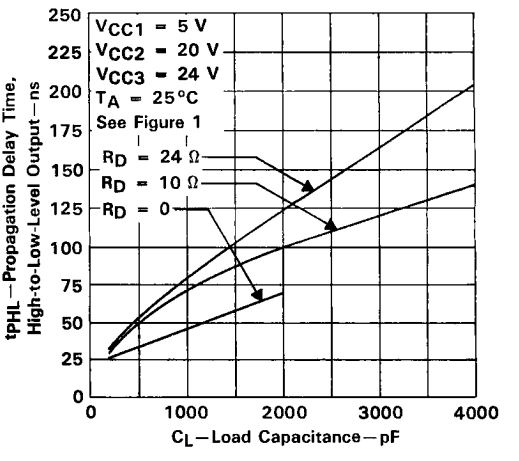


FIGURE 11

POWER DISSIPATION (ALL DRIVERS)
vs
FREQUENCY

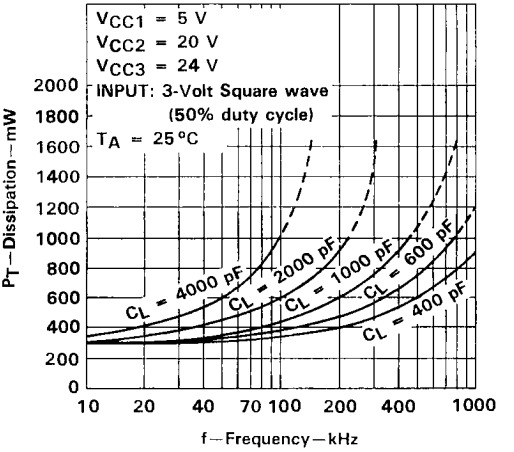


FIGURE 12

NOTE: For R_D = 0, operation with C_L > 2000 pF violates absolute maximum current rating.

APPLICATIONS INFORMATION

driving power MOSFETs

The drive requirements of power MOSFETs are much lower than comparable bipolar power transistors. The input impedance of a FET consists of a reverse biased PN junction that can be described as a large capacitance in parallel with a very high resistance. For this reason, the commonly used open-collector driver with a pull-up resistor is not satisfactory for high-speed applications. In Figure 13(a), an IRF151 power MOSFET switching an inductive load is driven by an open-collector transistor driver with a 470-Ω pull-up resistor. The input capacitance (C_{iss}) specification for an IRF151 is 4000 pF maximum. The resulting long turn-on time due to the product of input capacitance and the pull-up resistor is shown in Figure 13(b).

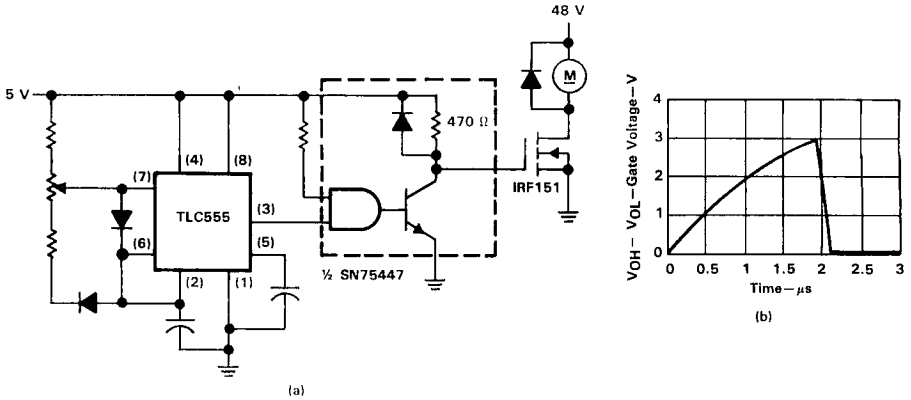


FIGURE 13. POWER MOSFET DRIVE USING SN75447

A faster, more efficient drive circuit uses an active pull-up as well as an active pull-down output configuration, referred to as a totem-pole output. The SN75374 driver provides the high-speed totem-pole drive desired in an application of this type, see Figure 14(a). The resulting faster switching speeds are shown in Figure 14(b).

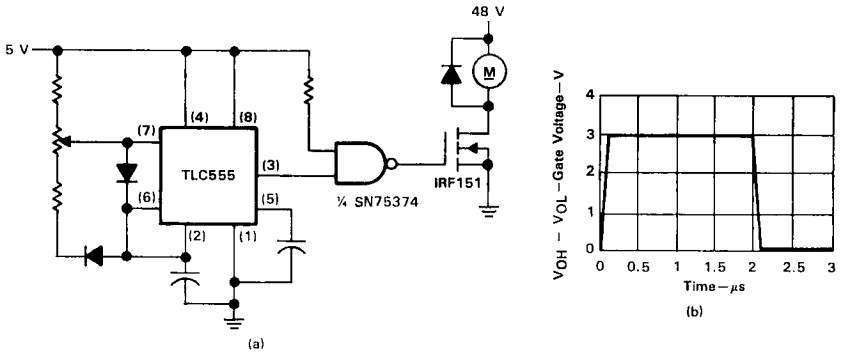


FIGURE 14. POWER MOSFET DRIVE USING SN75374

APPLICATIONS INFORMATION

Power MOSFET drivers must be capable of supplying high peak currents to achieve fast switching speeds as shown by the equation

$$I_{pk} = \frac{VC}{t_r}$$

where C is the capacitive load, and t_r is the desired rise time. V is the voltage that the capacitance is charged to. In the circuit shown in Figure 14(a), V is found by the equation

$$V = V_{OH} - V_{OL}$$

Peak current required to maintain a rise time of 100 ns in the circuit of Figure 14(a) is

$$I_{PK} = \frac{(3\text{-}0)4(10^{-9})}{100(10^{-9})} = 120 \text{ mA}$$

Circuit capacitance can be ignored because it is very small compared to the input capacitance of the IRF151. With a V_{CC} of 5 V, and assuming worst-case conditions, the gate drive voltage is 3 V.

For applications in which the full voltage of V_{CC2} must be supplied to the MOSFET gate, V_{CC3} should be at least 3 V higher than V_{CC2}.

THERMAL INFORMATION

power dissipation precautions

Significant power may be dissipated in the SN75374 driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. Figure 12 shows the power dissipated in a typical SN75374 as a function of frequency and load capacitance. Average power dissipated by this driver is derived from the equation

$$P_{T(AV)} = P_{DC(AV)} + P_{C(AV)} + P_{S(AV)}$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load and all are averaged over a full cycle.

The power components per driver channel are

$$P_{DC(AV)} = \frac{P_H t_H + P_L t_L}{T}$$

$$P_{C(AV)} \approx C V^2_C f$$

$$P_{S(AV)} = \frac{p_{LH} t_{LH} + P_{HL} t_{HL}}{T}$$

where the times are as defined in Figure 15.

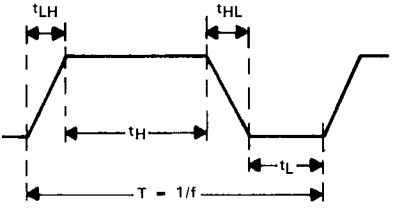


FIGURE 15. OUTPUT VOLTAGE WAVEFORM

THERMAL INFORMATION

P_L, P_H, P_{LH}, and P_{HL} are the respective instantaneous levels of power dissipation, C is the load capacitance. V_C is the voltage across the load capacitance during the charge cycle shown by the equation

$$V_C = V_{OH} - V_{OL}$$

$P_{S(AV)}$ may be ignored for power calculations at low frequencies.

In the following power calculation, all four channels are operating under identical conditions: f = 0.2 MHz, V_{OH} = 19.9 V and V_{OL} = 0.15 V with V_{CC1} = 5 V, V_{CC2} = 20 V, V_{CC3} = 24 V, V_C = 19.75 V, C = 1000 pF, and the duty cycle = 60%. At 0.2 MHz for C_L < 2000 pF, $P_{S(AV)}$ is negligible and can be ignored. When the output voltage is low, I_{CC2} is negligible and can be ignored.

On a per-channel basis using data sheet values

$$P_{DC(AV)} = \left[(5\text{ V})\left(\frac{4\text{ mA}}{4}\right) + (20\text{ V})\left(\frac{-2.2\text{ mA}}{4}\right) + (24\text{ V})\left(\frac{2.2\text{ mA}}{4}\right)\right](0.6) + \left[(5\text{ V})\left(\frac{31\text{ mA}}{4}\right) + (20\text{ V})\left(\frac{0\text{ mA}}{4}\right) + (24\text{ V})\left(\frac{16\text{ mA}}{4}\right)\right](0.4)$$

$P_{DC(AV)}$ = 58.2 mW per channel

Power during the charging time of the load capacitance is

$$P_{C(AV)} = (1000\text{ pF})(19.75\text{ V})^2(0.2\text{ MHz}) = 78\text{ mW per channel}$$

Total power for each driver is

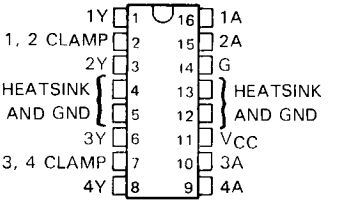
$$P_{T(AV)} = 58.2\text{ mW} + 78\text{ mW} = 136.2\text{ mW}$$

The total package power is

$$P_{T(AV)} = (136.2)(4) = 544.8\text{ mW}$$

- Saturating Outputs With Low On Resistance
- Very Low Standby Power . . . 53 mW Max
- High-Impedance MOS- or TTL-Compatible Inputs
- Standard 5-V Supply Voltage
- No Output Glitch During Power-Up or Power-Down
- Output Clamp Diodes for Transient Suppression
- 2-W Power Package . . . 60 °C/W $R_{\theta JA}$
- 600-mA Output Current
- 35-V Switching Voltage

NE DUAL-IN-LINE PACKAGE
(TOP VIEW)



FUNCTION TABLE
(EACH NAND DRIVER)

INPUTS		OUTPUT
A	G	Y
L	X	H
X	L	H
H	H	L

H = high level, L = low level
X = irrelevant

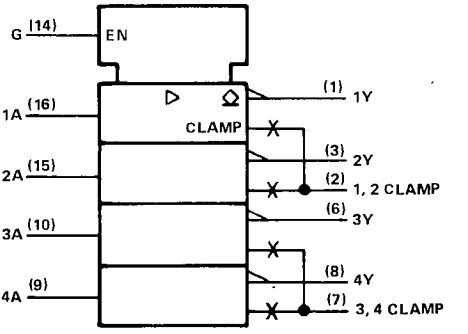
description

The SN75435 quadruple peripheral driver is designed for use in systems requiring high current, high voltage, and high load power. It features four inverting open-collector drivers with a common enable input that, when taken low, disables all four outputs. Each driver is protected against load shorts with its own latching over-current shutdown circuitry, which will turn the output off when a load short is detected. A short on one load will not affect operation of the other three drivers. The latch for the shutdown will hold the output off until the input or enable pin is taken low and then high again. A delay circuit is incorporated in the over-current shutdown to allow load capacitance of up to 5 nF at 35 V.

Applications include relay drivers, lamp drivers, solenoid drivers, motor drivers, LED drivers, line drivers, logic buffers, hammer drivers, and memory drivers.

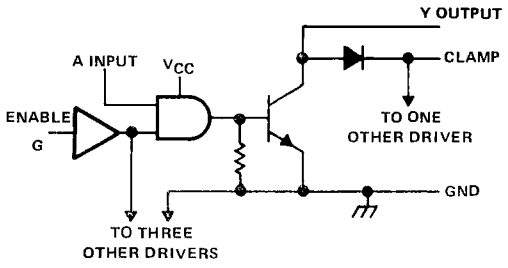
The SN75435 is characterized for operation from 0 °C to 70 °C.

logic symbol†

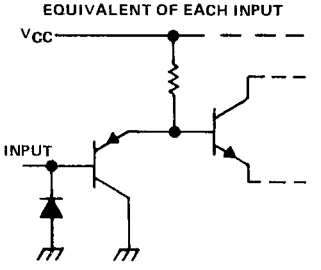


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematic of inputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range of V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Output supply voltage . . . . . 70 V
Output diode clamp current . . . . . 1 A
Continuous total power dissipation
at (or below) 25°C free-air temperature (see Note 2) . . . . . 2075 mW
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 16.6 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Output voltage			35	V
Output current			[illegible]	mA
Load capacitance (See Figure 3)			35	nF
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range

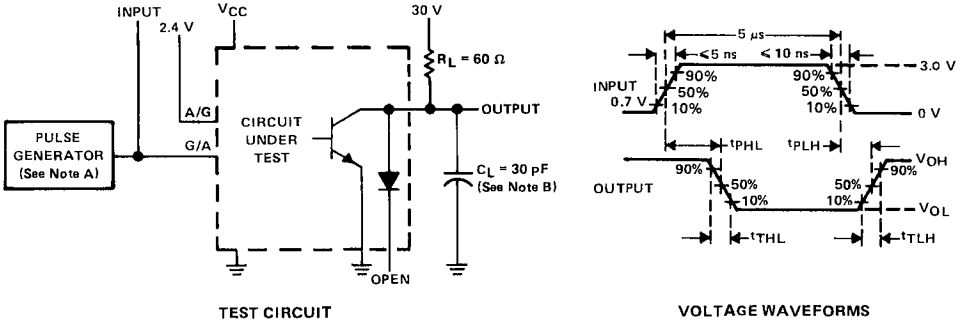
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V,	I_I = −12 mA		−0.9	−1.5	V
I_{OH}	High-level output current	V_{CC} = 4.75 V, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 70 V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IH} = 2 V	I_{OL} = 300 mA		0.25	0.5	V
			I_{OL} = 600 mA		0.55	1	
V_R	Output clamp diode reverse voltage	V_{CC} = 4.75 V,	I_R = [illegible] μA	70	100		V
V_F	Output clamp diode forward voltage	I_F = 600 mA			1.2	1.6	V
I_{IH}	High-level input current	V_{CC} = 5.25 V,	V_I = 5.25 V		0.01	10	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V,	V_I = 0.8 V		−0.5	−10	μA
	Over-current shutdown current	V_{CC} = 4.75 V to 5.25 V		650			mA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V,	V_I = 0		[illegible]	10	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V,	V_I = 5 V		55	75	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propogation delay time, low-to-high-level output	C_L = 30 pF, R_L = 60 Ω, See Figure 1		750		ns
t_{PHL}	Propagation delay time, high-to-low-level output			750		ns
t_{TLH}	Transition time, low-to-high-level output			200		ns
t_{THL}	Transition time, high-to-low-level output			200		ns
V_{OH}	High-level output voltage after switching	See Figure 2	V_S – 10			mV

PARAMETER MEASUREMENT INFORMATION

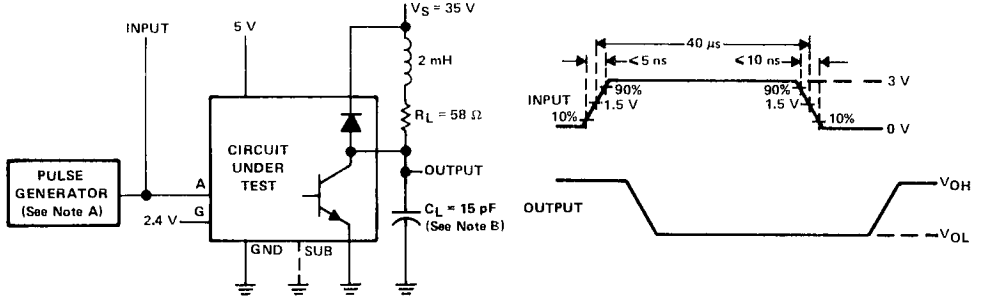


TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 100 kHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING CHARACTERISTICS

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50 Ω.
B. C_L include probe and jig capacitance.

FIGURE 2. LATCH-UP TEST

RECOMMENDED OPERATING CONDITIONS

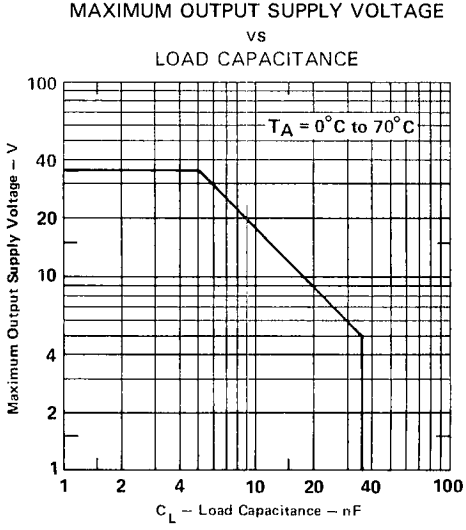
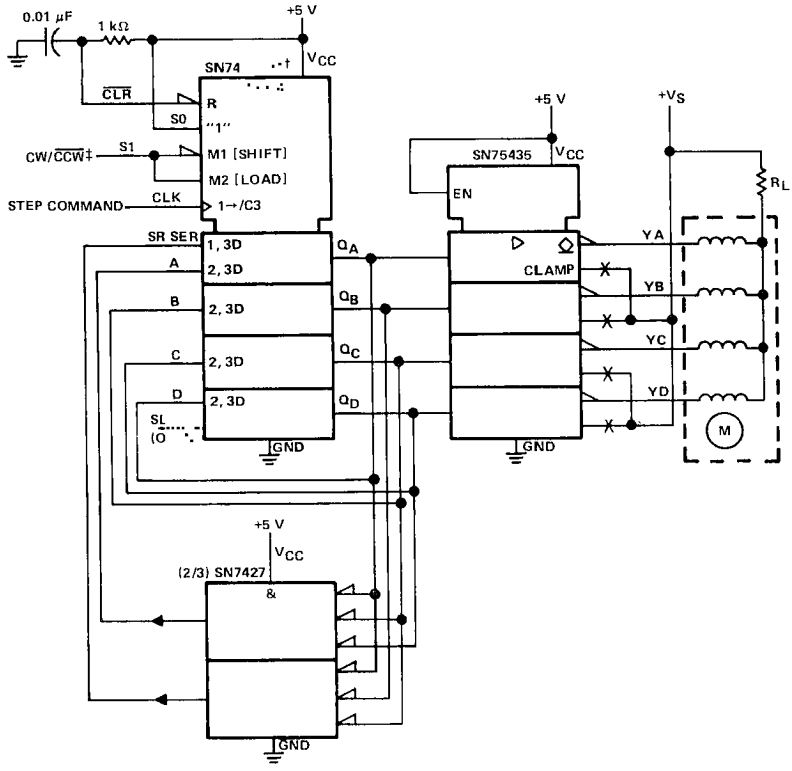
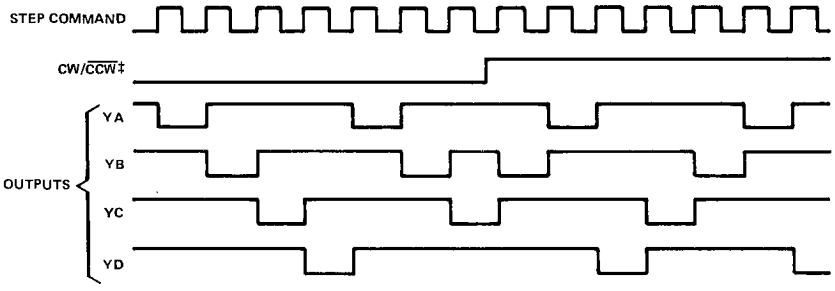


FIGURE 3

APPLICATION INFORMATION



4-WINDING STEPPER MOTOR CONTROL CIRCUIT



TIMING DIAGRAM FOR MDTOR CONTROL CIRCUIT

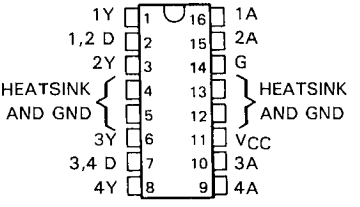
†The SN74LS194 is a universal shift register with both shift-right and shift-left capability. In this application S0 (pin 9) is wired high and only the shift-right and parallel-load modes are utilized. The logic symbol shown above has been simplified to show only the utilized modes.

‡This signal is CW/$\overline{\text{CCW}}$ or $\overline{\text{CW}}$/CCW depending on motor winding.

D2806, DECEMBER 1986

- Saturating Outputs With Low On-State Resistance
- High-Impedance Inputs Compatible With CMOS, MOS, and TTL Levels
- Very Low Standby Power . . 21 mW Maximum
- High-Voltage Outputs . 70 V Min
- No Output Glitch During Power Up or Power Down
- No Latch-Up Within Recommended Operating Conditions
- Output Clamp Diodes for Transient Suppression
- 2-W Power Package

NE PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each NAND driver)

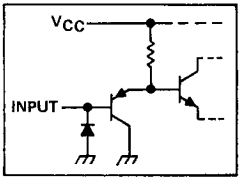
INPUTS		OUTPUT
A	G	Y
H	H	L
L	X	H
X	L	H

H = high level,
L = low level,
X = irrelevant

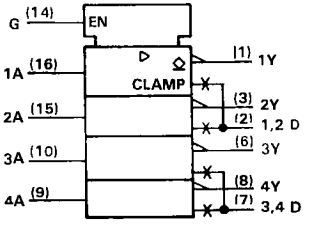
description

The SN75436, SN75437A, and SN75438 quadruple peripheral drivers are designed for use in systems requiring high current, high voltage, and high load power. Each device features four inverting open-collector outputs with a common enable input that, when taken low, disables all four outputs. The envelope of I-V characteristics exceeds the specifications sufficiently to avoid high-current latch-up. Applications include driving relays, lamps, solenoids, motors, LEDs, transmission lines, hammers, and other high-power-demand devices.

equivalent schematic of each input

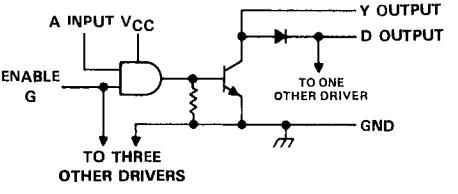


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic, each driver)



SELECTION GUIDE

FEATURE	SN75436	SN75437A	SN75[illegible]	[illegible]
Maximum recommended output current	0.5	0.5	[illegible]	[illegible]
Maximum V_{OL} at maximum I_{OL}	0.5	0.5	1	V
Maximum recommended output supply voltage in an inductive switching circuit, V_S	50	35	35	V

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 30 V
Output current: SN75436, SN75437A (see Note 1) . . . . . 0.75 A
SN75438 . . . . . 1.25 A
Output clamp diode current . . . . . 1.25 A
Output voltage (off-state) . . . . . 70 V
Continuous total power dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 2075 mW
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16-inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All four sections of these circuits may conduct rated current simultaneously; however, power dissipation average over a short time interval must fall within the continuous dissipation ratings.
2. For operation above 25°C free-air temperature, derate linearly to 1328 mW at 70°C at the rate of 16.6 mW/°C.

recommended operating conditions

PARAMETER	SN75436			SN75437A			SN75438			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	V
Output current, I_{OL}			0.5			0.5			1	A
Output supply voltage in inductive switching circuit (see Figure 2), V_S			50			35			35	V
High-level input voltage, V_{IH}	2			2			2			V
Low-level input voltage, V_{IL}			0.8			0.8			0.8	V
Operating free-air temperature, T_A	0		70	0		70	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

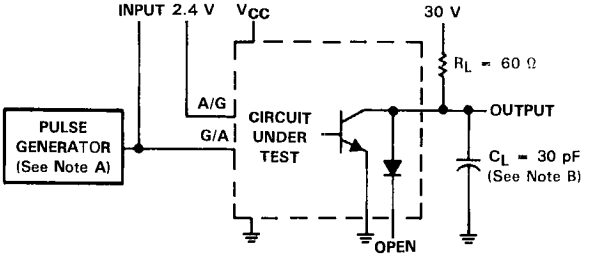
PARAMETER		TEST CONDITIONS		SN75436 SN75437A			SN75438			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	Input clamp	V_{CC} = 4.75 V,	I_I = −12 mA		−0.9	−1.5		−0.9	−1.5	V
I_{OH}	High-level output current	V_{CC} = 4.75 V, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 70 V		1	100		1	100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IH} = 2 V	I_{OL} = [illegible] mA		0.14	0.25		0.14	0.25	V
			I_{OL} = [illegible] mA		0.28	0.5		0.28	0.5	
			I_{OL} = 750 mA					0.42	0.75	
			I_{OL} = 1 A					0.60	1	
$V_{R(K)}$	Output clamp diode reverse voltage	V_{CC} = 4.75 V,	I_R = 100 μA	70	100		70	100		V
$V_{F(K)}$	Output clamp diode forward voltage	I_F = 500 mA			1	1.6		1	1.6	V
		I_F = 1 A						1.2	2	
I_{IH}	High-level input current	V_{CC} = 5.25 V,	V_I = 5.25 V		0.1	10		0.1	10	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V,	V_I = 0.8 V		−0.25	−10		−0.25	−10	μA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V,	V_I = 0		1	4		1	4	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V,	V_I = 5 V		45	65		45	65	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

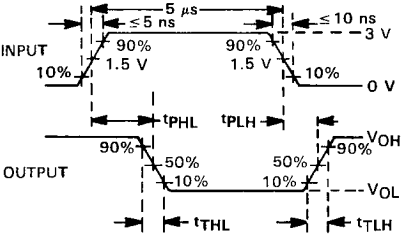
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		C_L = 30 pF, R_L = 60 Ω, See Figure 1		1950	5000	ns
t_{PHL}	Propagation delay time, high-to-low-level output				150	500	ns
t_{TLH}	Transition time, low-to-high-level output				40		ns
t_{THL}	Transition time, high-to-low-level output				36		ns
V_{OH}	High-level output voltage, after switching	SN75436	V_S = 50 V, R_L = 100 Ω, I_O ≈ 500 mA, See Figure 2	V_S – 10			mV
		SN75437A	V_S = 35 V, R_L = 70 Ω, I_O ≈ 500 mA, See Figure 2	V_S – 10			mV
		SN75438	V_S = 35 V, R_L = 35 Ω, I_O ≈ 1 A, See Figure 2	V_S – 10			mV

PARAMETER MEASUREMENT INFORMATION



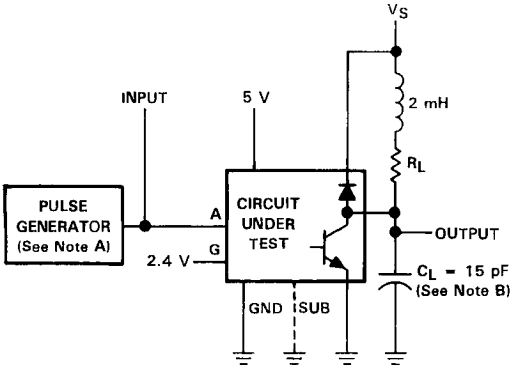
TEST CIRCUIT



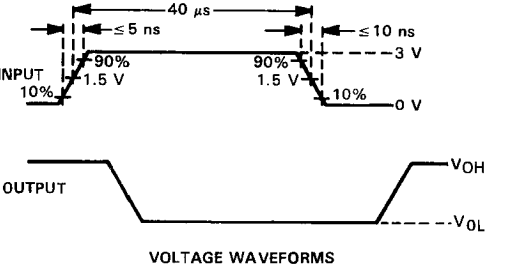
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 100 kHz, Z_o = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING CHARACTERISTICS



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_o = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 2. LATCH-UP TEST

PARAMETER MEASUREMENT INFORMATION

MAXIMUM COLLECTOR CURRENT
vs
DUTY CYCLE

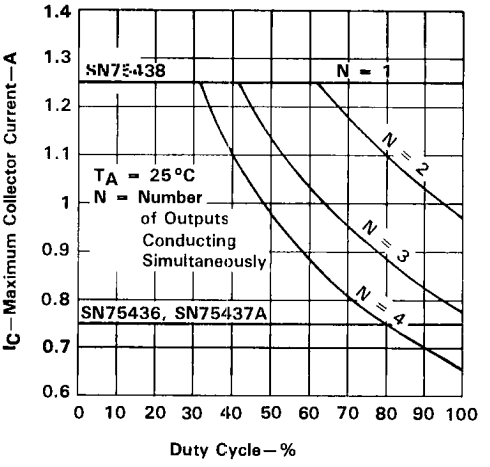


FIGURE 3

MAXIMUM COLLECTOR CURRENT
vs
DUTY CYCLE

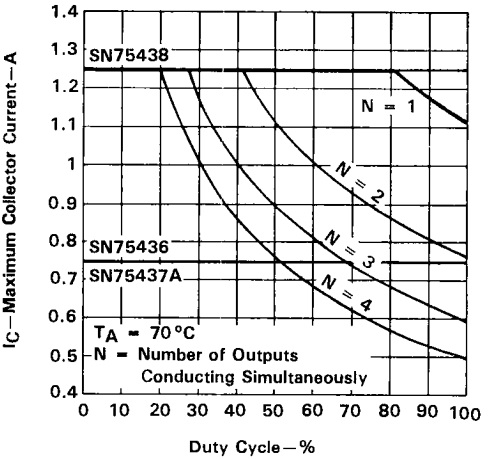


FIGURE 4

APPLICATION INFORMATION

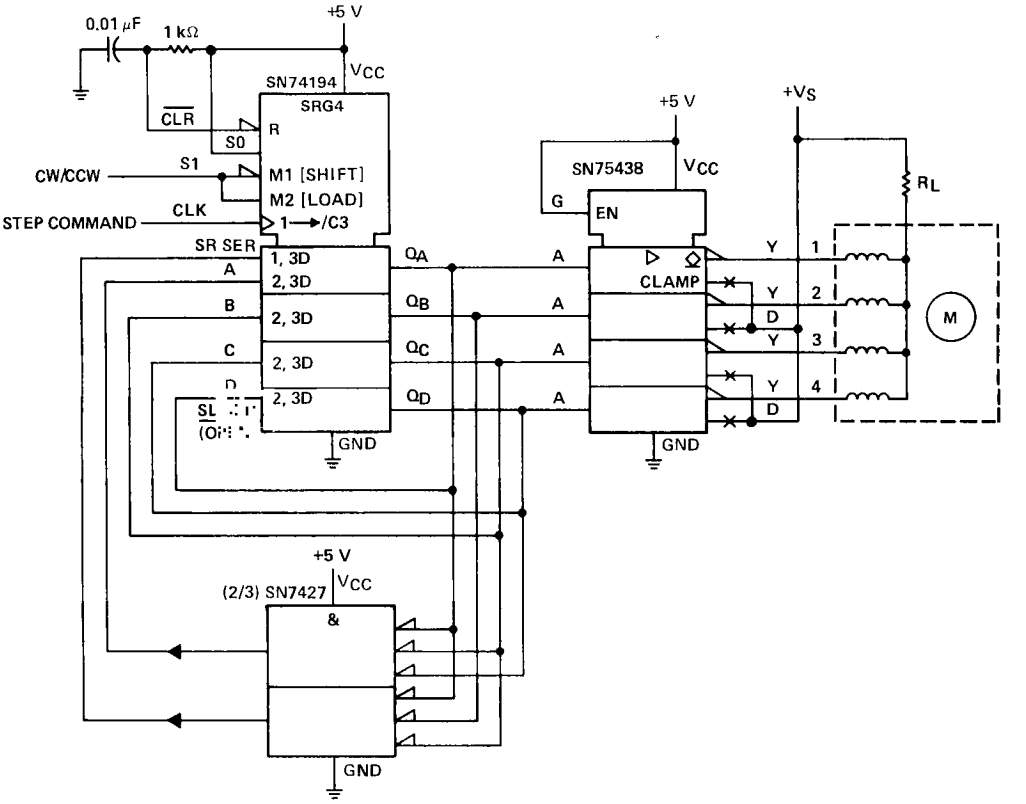


FIGURE 5. 4-WINDING STEPPER MOTOR CONTROL CIRCUIT

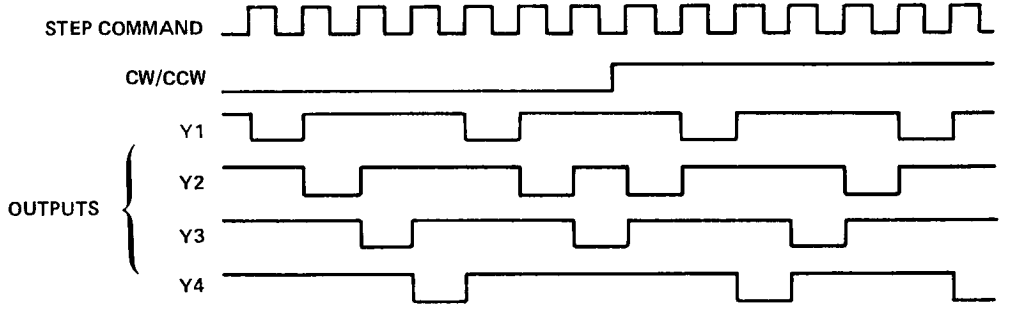
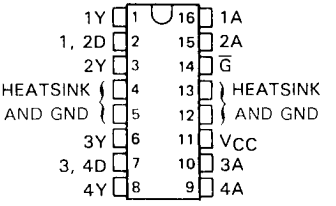


FIGURE 6. TIMING DIAGRAM

D3116, MAY 1988 – REVISED NOVEMBER 1989

- 1.3-A Current Capability Each Channel
- Saturating Outputs With Low On-State Resistance
- Two Inverting and Two Noninverting Driver Channels With Common Active-Low Enable Input
- Key Application Is as a Complete Full-Step 4-Phase DC Stepper Motor Driver Using Only Three Directly Connected Logic Control Signal Lines From Standard Microprocessors
- High-Impedance Inputs Compatible With TTL or CMOS Levels
- Very Low Standby Power . . . 10 mW Typ
- 50-V Noninductive Switching Voltage Capability
- 40-V Inductive Switching Voltage Capability
- Output Clamp Diodes for Inductive Transient Protection
- 2-W Power Package

NE PACKAGE
(TOP VIEW)



FUNCTION TABLES
(Each Channel 1 or Channel 4 Driver)

INPUTS		OUTPUT
A	$\overline{G}$	Y
H	L	L
L	X	H
X	H	H

(Each Channel 2 or Channel 3 Driver)

INPUTS		OUTPUT
A	$\overline{G}$	Y
L	L	L
H	X	H
X	H	H

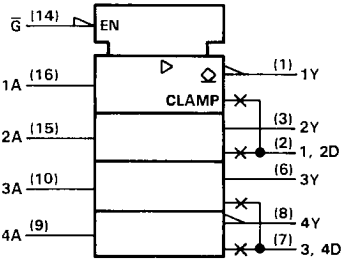
H = high level
L = low level
X = irrelevant

description

The SN75439 quadruple peripheral driver is designed for use in systems requiring high current, high voltage, and high load power. The device features two inverting and two noninverting open-collector outputs with a common-enable input that, when taken high, disables all four outputs. By pairing each inverting channel with a corresponding noninverting channel (such as channel 1 paired with channel 2 and channel 3 paired with channel 4), the device may be used as a complete full-step 4-phase dc stepper motor driver using only two input logic control signals plus the enable signal, as shown in Figure 3. Other applications include driving relays, lamps, solenoids, motors, LEDs, transmission lines, hammers, and other high-power-demand loads.

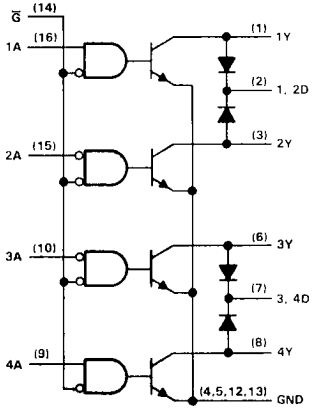
The SN75439 is characterized for operation from 0°C to 70°C.

logic symbol†

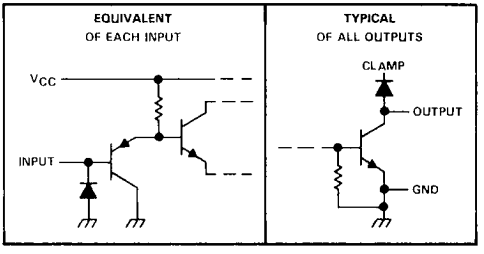


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.3 V to 7 V
Input voltage, V_I . . . . . 7 V
Output voltage range, V_O . . . . . −0.3 V to 52 V
Output voltage, V_O (inductive load) . . . . . 43 V
Output clamp-diode terminal voltage range, V_{OK} . . . . . −0.3 V to 52 V
Input current, I_I . . . . . −15 mA
Peak sink output current, I_{OM} (nonrepetitive, $t_w \leq 0.1$ ms) (see Note 2) . . . . . 1.5 A
(repetitive, $t_w \leq 10$ ms, duty cycle $\leq 50\%$) . . . . . 1.4 A
Continuous sink output current, I_O (see Note 2) . . . . . 1.3 A
Peak output clamp diode current, I_{OKM} (nonrepetitive, $t_w \leq 0.1$ ms) (see Note 2) . . . . . 1.5 A
(repetitive, $t_w \leq 10$ ms, duty cycle $\leq 50\%$) . . . . . 1.3 A
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3) . . . . . 2075 mW
Continuous total dissipation at (or below) 65°C case temperature (see Note 3) . . . . . 5000 mW
Operating case or virtual junction temperature range . . . . . −55°C to 150°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values are with respect to the network ground terminal (unless otherwise specified).
2. All four channels of this device may conduct rated current simultaneously; however, power dissipation average over a short time interval must fall within the continuous dissipation range.
3. For operation above 25°C free-air temperature, derate linearly at the rate of 16.6 mW/°C. For operation above 65°C case temperature, derate linearly at the rate of 59 mW/°C. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Output supply voltage in inductive [illegible] (V_S [illegible] 2)			40	V
High-level input voltage, V_{IH}	2		5.25	V
Low-level input voltage, V_{IL}	−0.3†		0.8	V
Low-level output current, I_{OL}			1.3	A
Operating free-air temperature, T_A	0	25	70	°C

† The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels.

electrical characteristics over recommended ranges of operating free-air temperature and supply voltages (unless otherwise noted)

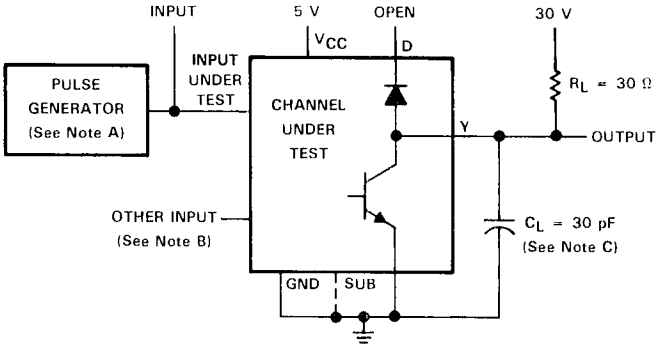
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −12 mA			−0.9	−1.5	V
V_{OL}	Low-level output voltage	I_{OL} = 0.5 A	See Note 4		0.2	0.35	V
		I_{OL} = 1 A			0.4	0.7	
		I_{OL} = 1.3 A			0.5	0.9	
$V_{F(K)}$	Output clamp diode forward voltage	I_F = 0.5 A	See Note 4		1.1	1.9	V
		I_F = 1 A			1.3	2.2	
		I_F = 1.3 A			1.4	2.4	
I_{OH}	High-level output current	V_{OH} = 50 V,	V_{OK} = 50 V			100	μA
I_{IH}	High-level input current	$V_I = V_{IH}$				10	μA
I_{IL}	Low-level input current	V_I = 0 to 0.8 V				−10	μA
$I_{R(K)}$	Output clamp-diode reverse current (at Y output)	V_R = 50 V,	V_O = 0			100	μA
I_{CC}	Supply current	All outputs at high level (off)			2	8	mA
		All outputs at low level (on)			140	200	
		Two outputs at high level (off) and two outputs at low level (on)			70	110	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 4: These parameters must be measured using pulse techniques, t_w = 1 ms, duty cycle ≤ 10%.

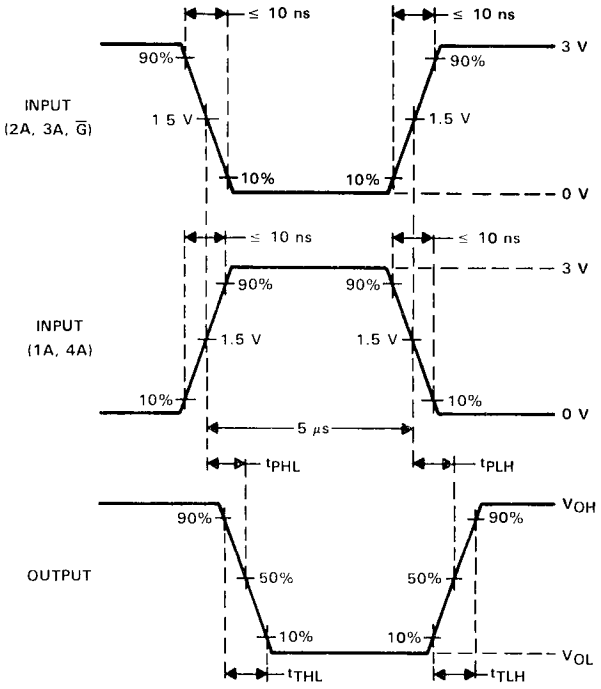
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	I_{OL} ≈ 1 A, R_L = 30 Ω,	C_L = 30 pF, See Figure 1		1500		ns
t_{PHL}	Propagation delay time, high-to-low-level output				100		ns
t_{TLH}	Transition time, low-to-high-level output				170		ns
t_{THL}	Transition time, high-to-low-level output				50		ns
V_{OH}	High-level output voltage (after switching inductive load)	V_S = 40 V, R_L = 31 Ω,	I_O ≈ 1.3 A, See Figure 2	V_S−100			mV

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

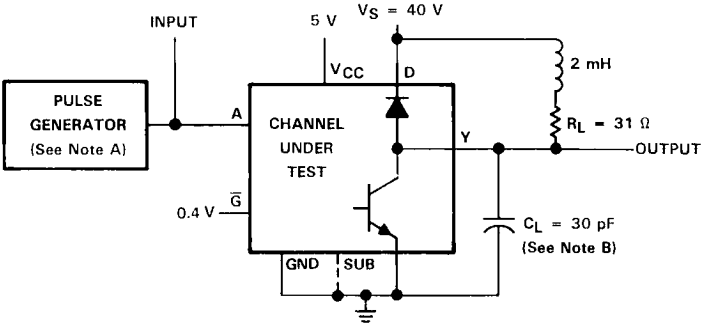


VOLTAGE WAVEFORMS

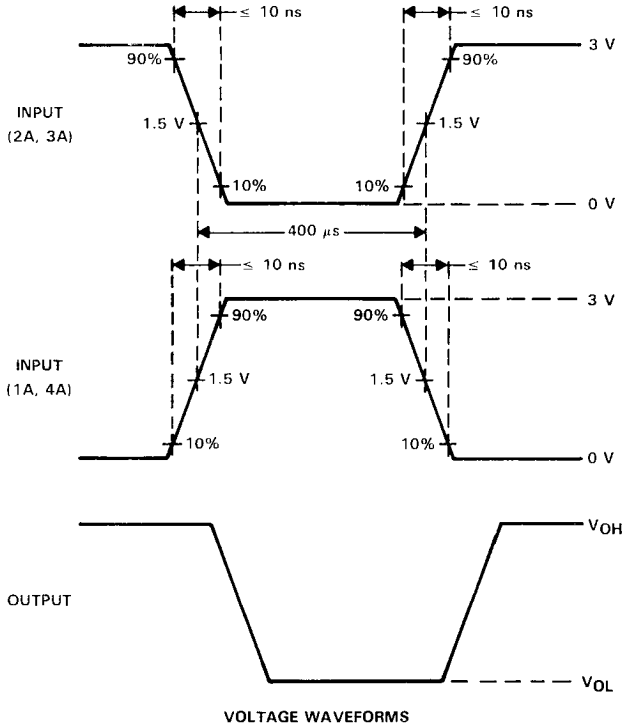
NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 1%, Z_O = 50 Ω.
B. Enable input $\overline{G}$ is at 0 V if input A is used as the switching input. When $\overline{G}$ is used as the switching input, the corresponding A input is at 0 V if testing channel 2 or channel 3 or at 3 V if testing channel 1 or channel 4.
C. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING CHARACTERISTICS

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 1%, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 2. OUTPUT LATCH-UP TEST

APPLICATION INFORMATION

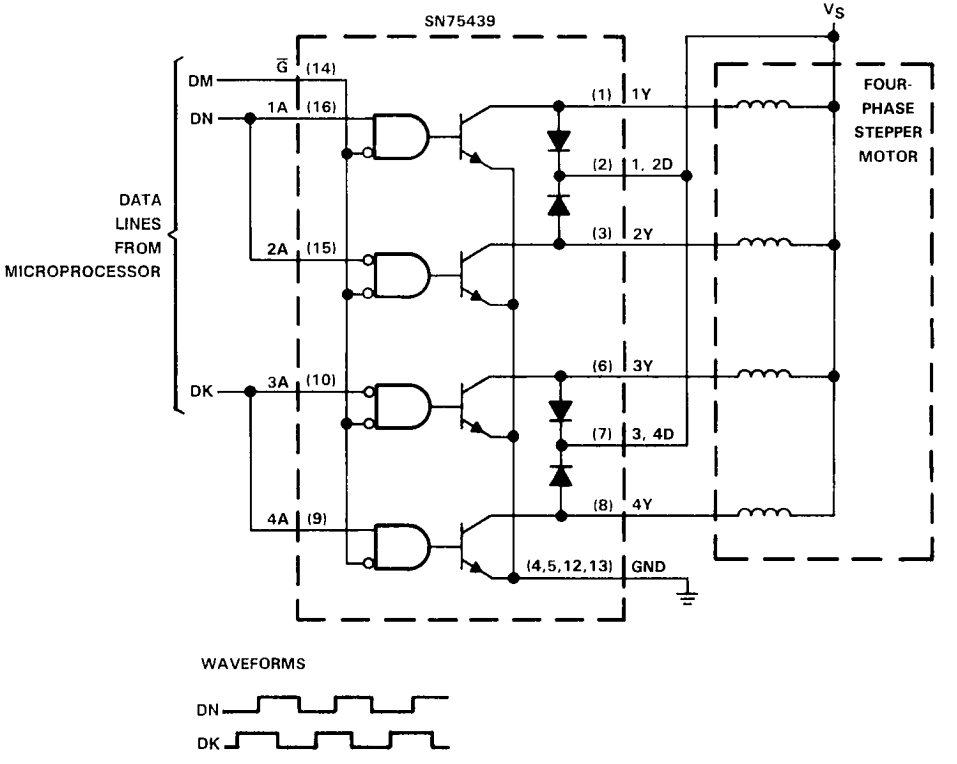


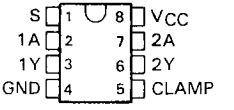
FIGURE 3. FULL-STEP FOUR-PHASE STEPPER MOTOR DRIVER

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

D2481, [illegible] 1978—REVISED DECEMBER 1989

- Very Low Power Requirements
- Very Low Input Current
- Characterized for Use to 350 mA
- No Output Latch-Up at 50 V (After Conducting 300 mA)
- High-Voltage Outputs (70 V Min)
- Output Clamp Diodes for Transient Suppression (350 mA, 70 V)
- TTL- or MOS-Compatible Diode-Clamped Inputs
- Standard Supply Voltage
- Suitable for Hammer-Driver Applications

D OR P PACKAGE
(TOP VIEW)

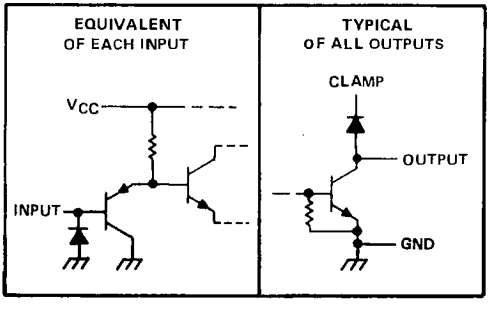


description

Series SN75446 dual peripheral drivers are designed for use in systems that require high current, high voltage, and fast switching times. The SN75446, SN75447, SN75448, and SN75449 provide AND, NAND, OR, and NOR drivers, respectively. These devices have diode-clamped inputs as well as high-current, high-voltage inductive-clamp diodes on the outputs.

Series SN75446 drivers are characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



FUNCTION TABLES

SN75446
(EACH AND DRIVER)

INPUTS		OUTPUT
A	S	Y
H	H	H
L	X	L
X	L	L

SN75447
(EACH NAND DRIVER)

INPUTS		OUTPUT
A	S	Y
H	H	L
L	X	H
X	L	H

SN75448
(EACH OR DRIVER)

INPUTS		OUTPUT
A	S	Y
H	X	H
X	H	H
L	L	L

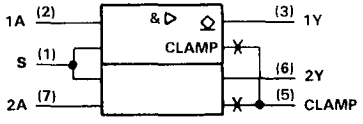
SN75449
(EACH NOR DRIVER)

INPUTS		OUTPUT
A	S	Y
H	X	L
X	H	L
L	L	H

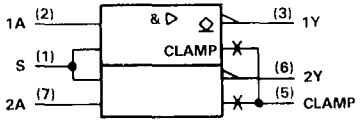
H = high level
L = low level
X = irrelevant

logic symbols†

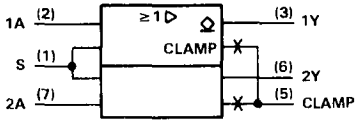
SN75446



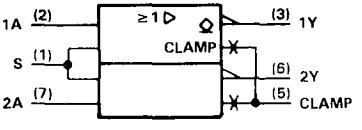
SN75447



SN75448



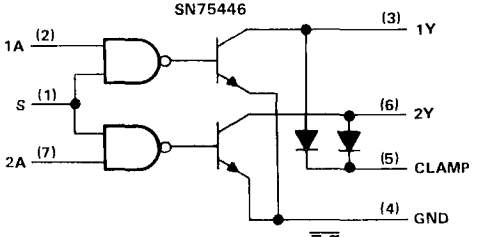
SN75449



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

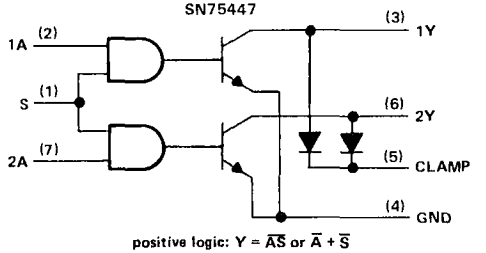
logic diagrams (positive logic)

SN75446



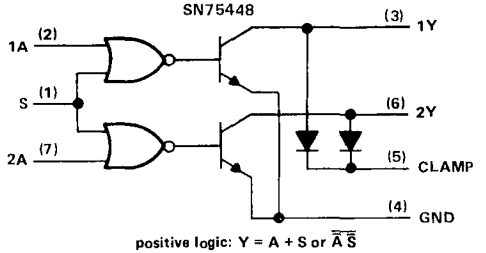
positive logic: $Y = AS$ or $\overline{\overline{A}+\overline{S}}$

SN75447



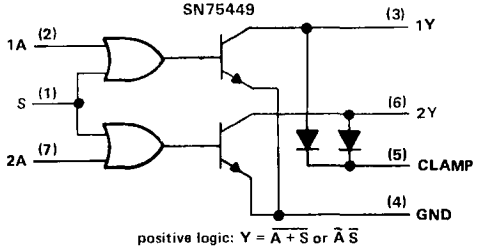
positive logic: $Y = \overline{AS}$ or $\overline{A} + \overline{S}$

SN75448



positive logic: $Y = A + S$ or $\overline{\overline{A}\,\overline{S}}$

SN75449



positive logic: $Y = \overline{\overline{A} + \overline{S}}$ or $\overline{A}\,\overline{S}$

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Output current (see Note 2) . . . . . 400 mA
Output clamp diode current . . . . . 400 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Both halves of this dual circuit may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation ratings.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Operating free-air temperature, T_A	0		70	°C

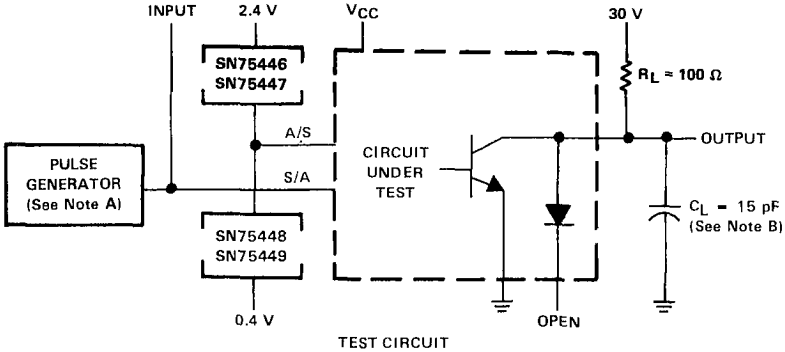
electrical characteristics over recommended operating free-air temperature range

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		$I_I = -12$ mA			−0.9	−1.5	V
I_{OH}	High-level output current		$V_{CC} = 4.75$ V, $V_{IL} = 0.8$ V,	$V_{IH} = 2$ V, $V_{OH} = 70$ V		1	100	μA
V_{OL}	Low-level output voltage		$V_{CC} = 4.75$ V, $V_{IH} = 2$ V, $V_{IL} = 0.8$ V	$I_{OL} = 100$ mA		0.10	0.3	V
				$I_{OL} = 200$ mA		0.22	0.45	
				$I_{OL} = 300$ mA		0.45	0.65	
				$I_{OL} = 350$ mA		0.55	0.75	
$V_{(BR)O}$	Output breakdown voltage		$V_{CC} = 4.75$ V,	$I_{OH} = 100$ μA	70			V
$V_{R(K)}$	Output clamp diode reverse voltage		$V_{CC} = 4.75$ V,	$I_R = 100$ μA	70			V
$V_{F(K)}$	Output clamp diode forward voltage		$V_{CC} = 4.75$ V,	$I_F = 350$ mA	0.6	1.2	1.6	V
I_{IH}	High-level input current		$V_{CC} = 5.25$ V,	$V_I = 5.25$ V		0.01	10	μA
I_{IL}	Low-level input current	A input	$V_{CC} = 5.25$ V,	$V_I = 0.8$ V		−0.5	−10	μA
		Strobe S				−1	−20	
I_{CCH}	Supply current, outputs high	SN75446	$V_{CC} = 5.25$ V	$V_I = 5$ V		11	18	mA
		SN75447		$V_I = 0$		11	18	
		SN75448		$V_I = 5$ V		18	25	
		SN75449		$V_I = 0$		18	25	
I_{CCL}	Supply current, outputs low	SN75446	$V_{CC} = 5.25$ V	$V_I = 0$		11	18	mA
		SN75447		$V_I = 5$ V		11	18	
		SN75448		$V_I = 0$		18	25	
		SN75449		$V_I = 5$ V		18	25	

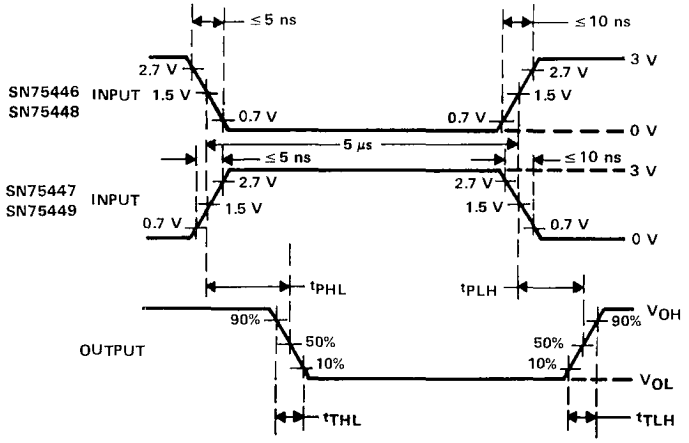
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 100 Ω, See Figure 1		300	750	ns
t_{PHL}	Propagation delay time, high-to-low-level output			200	500	ns
t_{TLH}	Transition time, low-to-high-level output			50	[illegible]	ns
t_{THL}	Transition time, high-to-low-level output			50	[illegible]	ns
V_{OH}	High-level output voltage after switching	V_S = 55 V, I_O = 300 mA, See Figure 2	V_S − 0.018			V

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

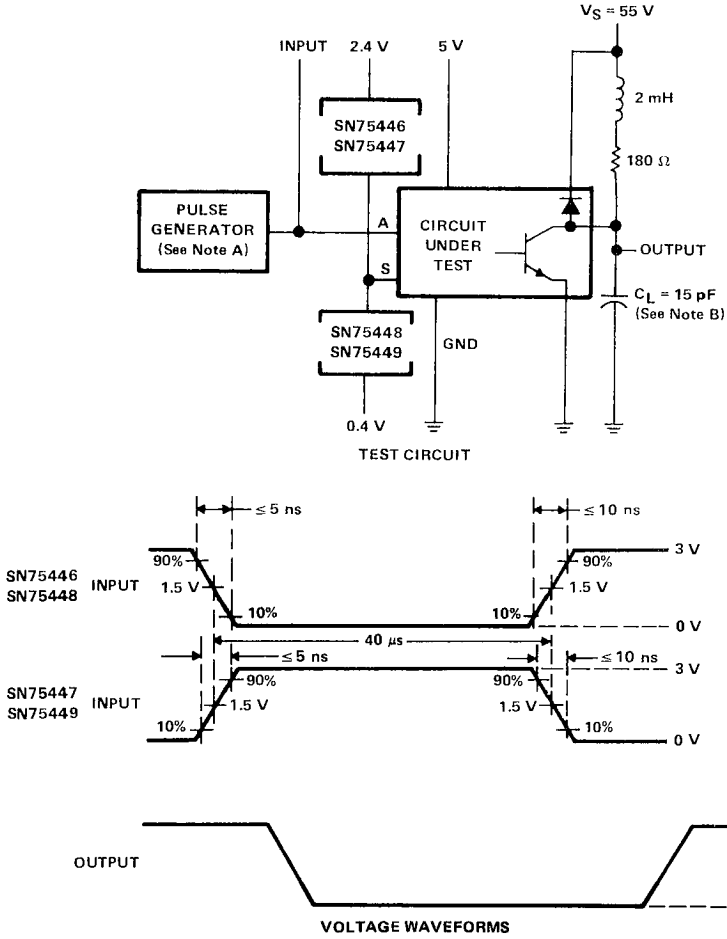


VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 100 kHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING CHARACTERISTICS

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

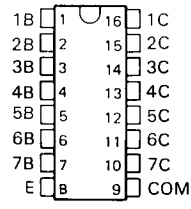
FIGURE 2. LATCH-UP TEST

D2625, DECEMBER 1976—REVISED SEPTEMBER 1986

HIGH VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

- 500-mA Rated Collector Current (Single Output)
- High-Voltage Outputs . . . 100 V
- Output Clamp Diodes
- Inputs Compatible with Various Types of Logic
- Relay Driver Applications
- Higher-Voltage Versions of ULN2005A, ULN2001A, ULN2002A, ULN2003A, and ULN2004A, Respectively, for Commercial Temperature Range

D OR N PACKAGE
(TOP VIEW)

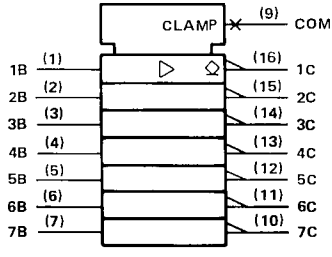


description

The SN75465, SN75466, SN75467, SN75468, and SN75469 are monolithic high-voltage, high-current Darlington transistor arrays. Each consists of seven n-p-n Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of each Darlington pair is 500 mA. The Darlington pairs may be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers.

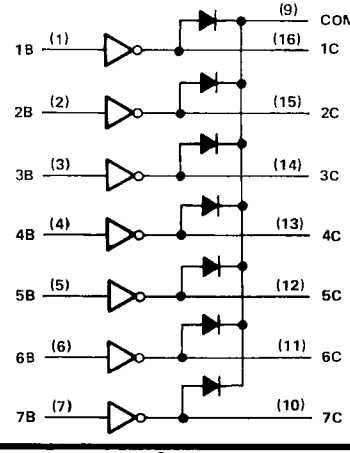
The SN75465 has a 1050-Ω series base resistor and is especially designed for use with TTL where higher current is required and loading of the driving source is not a concern. The SN75466 is a general-purpose array and may be used with TTL, P-MOS, CMOS, and other MOS technologies. The SN75467 is specifically designed for use with 14- to 25-V P-MOS devices and each input has a zener diode and resistor in series to limit the input current to a safe limit. The SN75468 has a 2700-Ω series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS. The SN75469 has a 10.5-kΩ series base resistor to allow its operation directly from CMOS or P-MOS that use supply voltages of 6 to 15 V. The required input current is below that of the SN75468 and the required voltage is less than that required by the SN75467.

logic symbol†

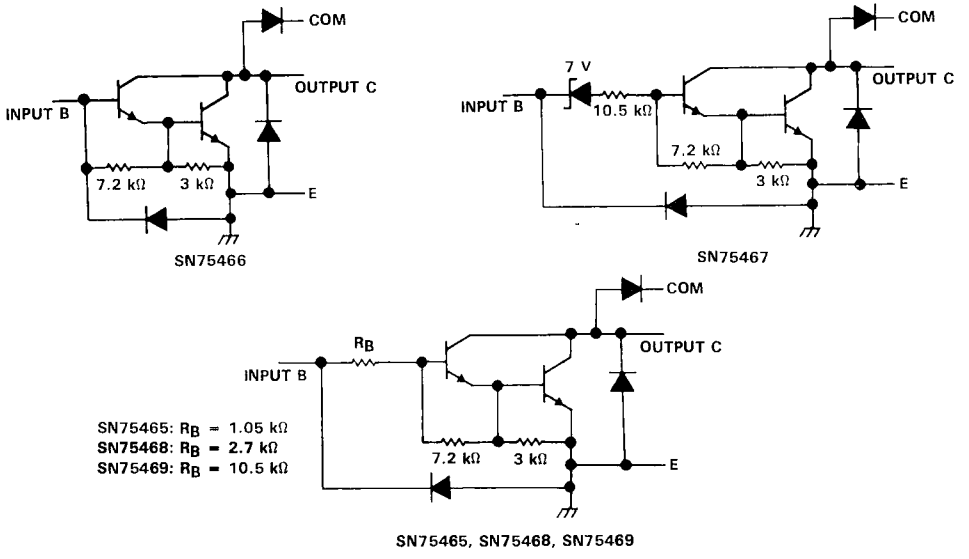


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



schematics (each Darlington pair)



All resistor values shown are nominal.

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Collector-emitter voltage	100 V
Input voltage (see Note 1): SN75465	15 V
SN75467, SN75468, SN75469	30 V
Peak collector current (see Figures 14 and 15)	500 mA
Output clamp diode current	500 mA
Total emitter-terminal current	−2.5 A
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: All voltage values are with respect to the emitter/substrate terminal, E, unless otherwise noted.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	736 mW

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS			SN75465			UNIT
						MIN	TYP	MAX	
I_{CEX}	Collector cutoff current	1	V_{CE} = 100 V,	I_I = 0				50	μA
			V_{CE} = 100 V,	I_I = 0,	T_A = 70°C			100	
$I_{I(off)}$	Off-state input current	3	V_{CE} = 100 V,	I_C = 500 μA,	T_A = 70°C	50	65		μA
I_I	Input current	4	V_I = 3 V				1.5	2.4	mA
$V_{I(on)}$	On-state input voltage	5	V_{CE} = 2 V,	I_C = 350 mA				2.4	V
$V_{CE(sat)}$	Collector-emitter saturation voltage	6	I_I = · μA,	I_C = 100 mA			0.9	1.1	V
			I_I = · μA,	I_C = 200 mA			1	1.3	
			I_I = 500 μA,	I_C = 350 mA			1.2	1.6	
I_R	Clamp diode reverse current	7	V_R = · V,					50	μA
			V_R = · V,	T_A = 70°C				100	
V_F	Clamp diode forward voltage	8	I_F = 350 mA				1.7	2	V
C_i	Input capacitance		V_I = 0,	f = 1 MHz			15	25	pF

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS			SN75466			SN75467			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
I_{CEX}	Collector cutoff current	1	V_{CE} = 100 V,	I_I = 0				50			50	μA
			V_{CE} = 100 V,	I_I = 0				100			100	
		2	T_A = 70°C	V_I = 6 V								
$I_{I(off)}$	Off-state input current	3	V_{CE} = 50 V, T_A = 70°C	I_C = 500 μA,		50	65		50	65		μA
I_I	Input current	4	V_I = 17 V							0.82	1.25	mA
h_{FE}	Static forward current transfer ratio	6	V_{CE} = 2 V,	I_C = 350 mA		1000						
$V_{I(on)}$	On-state input voltage	5	V_{CE} = 2 V,	I_C = 300 mA							13	V
$V_{CE(sat)}$	Collector-emitter saturation voltage	6	I_I = 250 μA,	I_C = 100 mA			0.9	1.1		0.9	1.1	V
			I_I = · μA,	I_C = · mA			1	1.3		1	1.3	
			I_I = · μA,	I_C = · mA			1.2	1.6		1.2	1.6	
I_R	Clamp diode forward voltage	7	V_R = · V					50			50	μA
			V_R = · V,	T_A = 70°C				100			100	
V_F	Clamp diode forward voltage	8	I_F = 350 mA				1.7	2		1.7	2	V
C_i	Input capacitance		V_I = 0,	f = 1 MHz			15	25		15	25	pF

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	SN75468 MIN	SN75468 TYP	SN75468 MAX	SN75469 MIN	SN75469 TYP	SN75469 MAX	UNIT
I_{CEX}	Collector cutoff current	1	V_{CE} = 100 V, I_I = 0			50			50	μA
			V_{CE} = 100 V, I_I = 0			100				
		2	T_A = 70°C, V_I = 1 V							
$I_{I(off)}$	Off-state input current	3	V_{CE} = 50 V, I_C = 500 μA, T_A = 70°C	50	65		50	65		μA
I_I	Input current	4	V_I = 3.85 V		0.93	1.35				mA
			V_I = 5 V					0.35	0.5	
			V_I = 12 V					1	1.45	
$V_{I(on)}$	On-state input voltage	5	V_{CE} = 2 V, I_C = 125 mA						5	V
			V_{CE} = 2 V, I_C = [illegible] mA			2.4			6	
			V_{CE} = 2 V, I_C = [illegible] mA			2.7				
			V_{CE} = 2 V, I_C = 275 mA						7	
			V_{CE} = 2 V, I_C = 300 mA			3				
			V_{CE} = 2 V, I_C = 350 mA						8	
$V_{CE(sat)}$	Collector-emitter saturation voltage	6	I_I = [illegible] μA, I_C = [illegible] mA		0.9	1.1		0.9	1.1	V
			I_I = [illegible] μA, I_C = [illegible] mA		1	1.3		1	1.3	
			I_I = 500 μA, I_C = 350 mA		1.2	1.6		1.2	1.6	
I_R	Clamp diode reverse current	7	V_R = 100 V			50			50	μA
			V_R = 100 V, T_A = 70°C			100			100	
V_F	Clamp diode forward voltage	8	I_F = 350 mA		1.7	2		1.7	2	V
C_i	Input capacitance		V_I = 0, f = 1 [illegible]		15	25		15	25	pF

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_S = 50 V, R_L = 163 Ω,		0.25	1	μs
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF, See Figure 9		0.25	1	μs
V_{OH}	High-level output voltage after switching	V_S = 50 V, I_O ≈ 300 mA, See Figure 10	V_S − 20			mV

PARAMETER MEASUREMENT INFORMATION

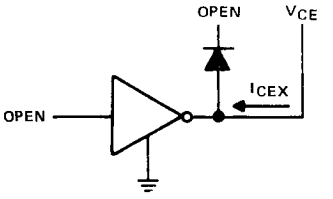


FIGURE 1. I_{CEX}

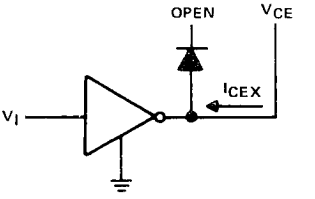


FIGURE 2. I_{CEX}

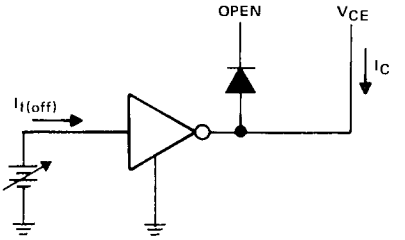


FIGURE 3. $I_{I(off)}$

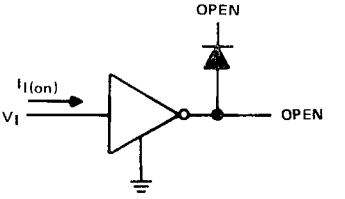


FIGURE 4. I_I

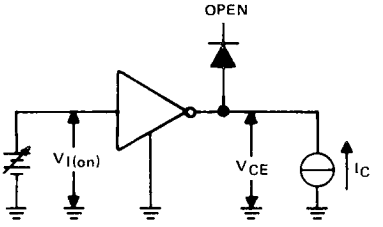
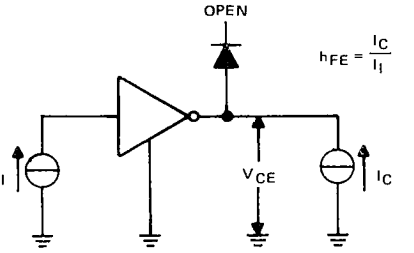


FIGURE 5. $V_{I(on)}$



NOTE: I_I is fixed for measuring $V_{CE(sat)}$, variable for measuring h_{FE}.

FIGURE 6. h_{FE}, $V_{CE(sat)}$

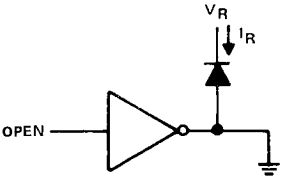


FIGURE 7. I_R

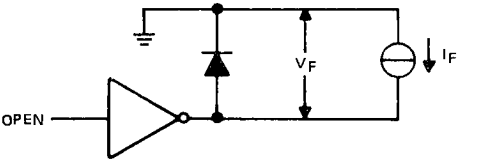
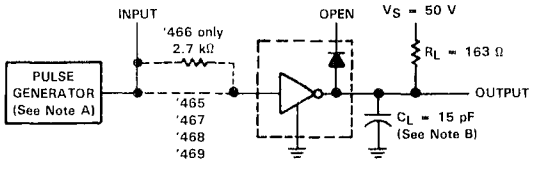
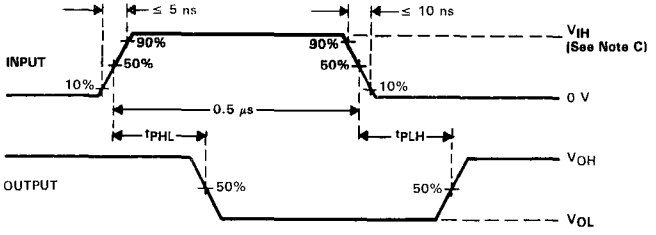


FIGURE 8. V_F

PARAMETER MEASUREMENT INFORMATION



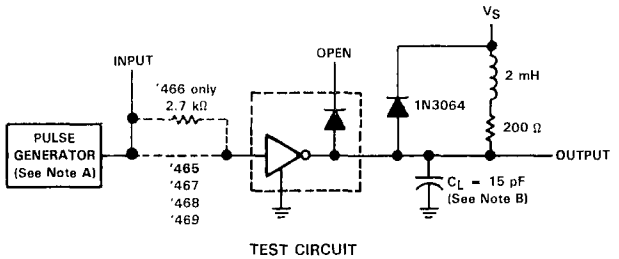
TEST CIRCUIT



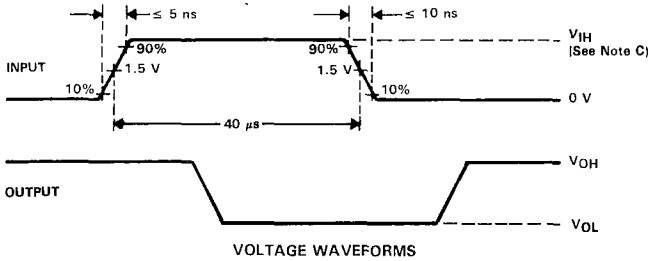
VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. For testing the '465, '466, and '468, V_{IH} = 3 V; for the '467, V_{IH} = 13 V; for the '469, V_{IH} = 8 V.

FIGURE 9. PROPAGATION DELAY TIMES



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. For testing the '465, '466, and '468, V_{IH} = 3 V; for the '467, V_{IH} = 13 V; for the '469, V_{IH} = 8 V.

FIGURE 10. LATCH-UP TEST

TYPICAL CHARACTERISTICS

COLLECTOR EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT (ONE DARLINGTON)

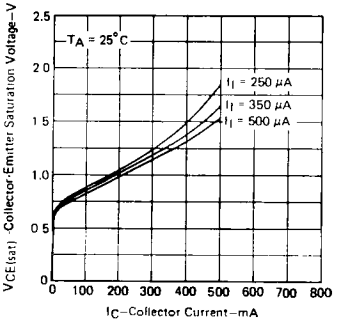


FIGURE 11

COLLECTOR EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT (TWO DARLINGTONS PARALLELED)

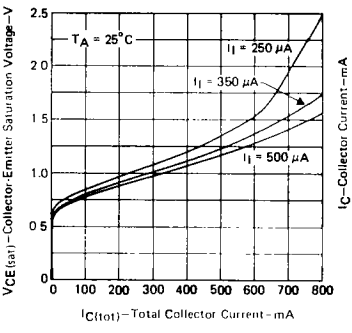


FIGURE 12

COLLECTOR CURRENT vs INPUT CURRENT

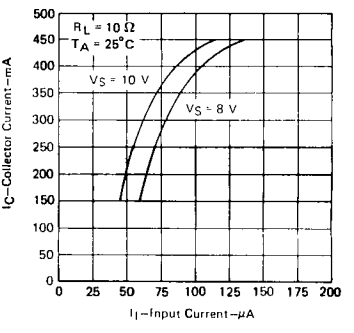


FIGURE 13

THERMAL INFORMATION

D PACKAGE MAXIMUM COLLECTOR CURRENT vs DUTY CYCLE

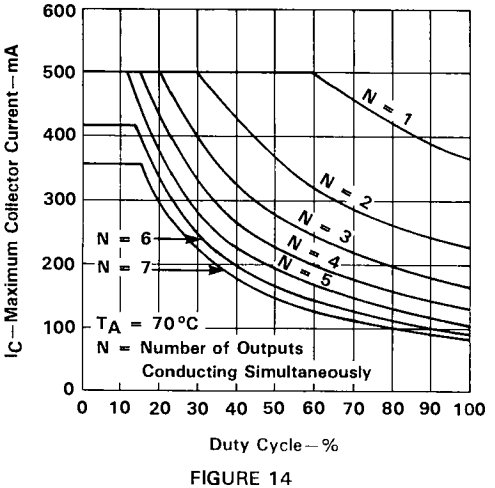


FIGURE 14

N PACKAGE MAXIMUM COLLECTOR CURRENT vs DUTY CYCLE

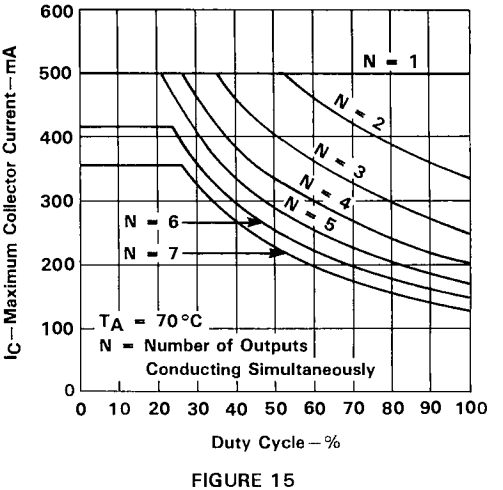
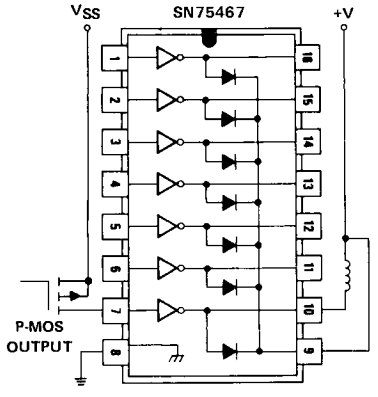
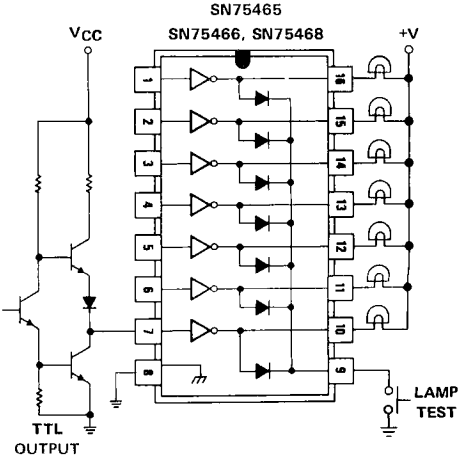


FIGURE 15

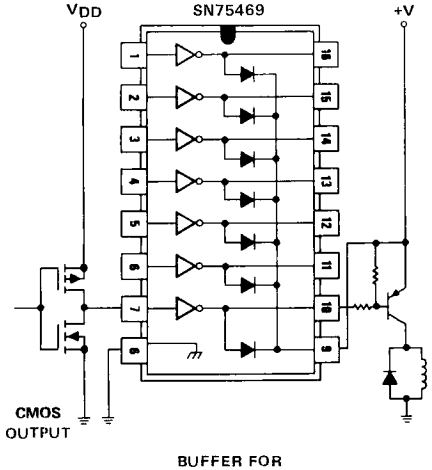
TYPICAL APPLICATION DATA



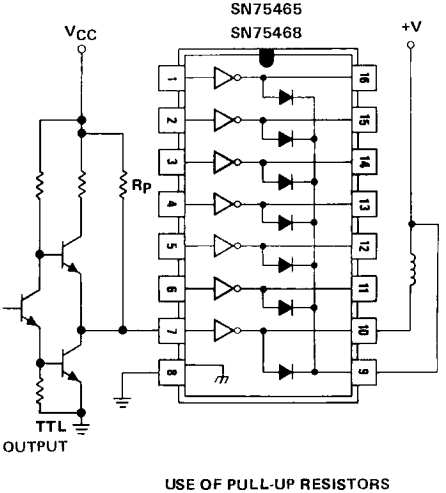
P-MOS TO LOAD



TTL TO LOAD



BUFFER FOR
HIGHER CURRENT LOADS



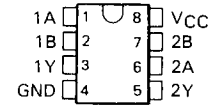
USE OF PULL-UP RESISTORS
TO INCREASE DRIVE CURRENT

D2130, DECEMBER 1976—REVISED MAY 1990

PERIPHERAL DRIVERS FOR HIGH-VOLTAGE, HIGH-CURRENT DRIVER APPLICATIONS

- Characterized for Use to 300 mA
- High-Voltage Outputs
- No Output Latch-Up at 55 V (After Conducting 300 mA)
- Medium-Speed Switching
- Circuit Flexibility for Varied Applications and Choice of Logic Function
- TTL-Compatible Diode-Clamped Inputs
- Standard Supply Voltages
- Plastic DIP (P) with Copper Lead Frame Provides Cooler Operation and Improved Reliability

D OR P PACKAGE
(TOP VIEW)



SUMMARY OF SERIES SN75471

DEVICE	LOGIC OF COMPLETE CIRCUIT	PACKAGES
SN75471	AND	D,P
SN75472	NAND	D,P
SN75473	OR	D,P

description

Series SN75471 dual peripheral drivers are functionally interchangeable with Series SN75451B and Series SN75461 peripheral drivers, but are designed for use in systems that require higher breakdown voltages than either of those series can provide at the expense of slightly slower switching speeds than Series 75451B (limits are the same as Series SN75461). Typical applications include logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers.

The SN75471, SN75472, and SN75473 are dual peripheral AND, NAND, and OR drivers, respectively, (assuming positive logic) with the output of the logic gates internally connected to the bases of the n-p-n output transistors.

Series SN75471 drivers are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Off-state output voltage . . . . . 70 V
Continuous collector or output current (see Note 3) . . . . . 400 mA
Peak collector or output current ($t_w \leq 10$ ms, duty cycle $\leq 50\%$, see Note 3) . . . . . 500 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to the network ground terminal unless otherwise specified.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

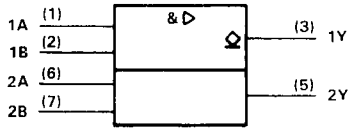
DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Operating free-air temperature, T_A	0		70	°C

logic symbol†



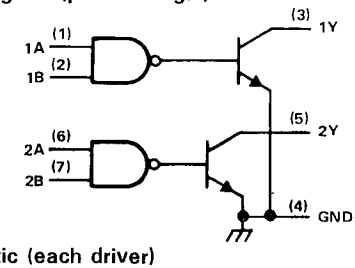
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE
(EACH DRIVER)

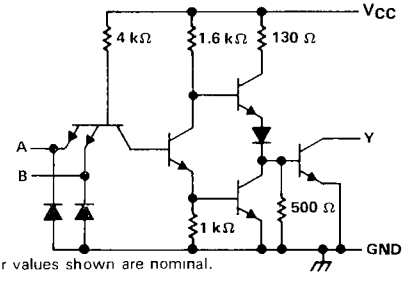
A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

positive logic:
$Y = AB$ or $\overline{\overline{A} + \overline{B}}$

logic diagram (positive logic)



schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

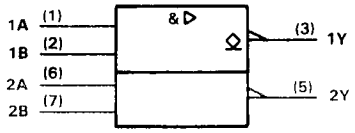
PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V, I_I = −12 mA		−1.2	−1.6	V
I_{OH}	High-level output current	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{OH} = 70 V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.4	V
		V_{CC} = 4.75 V, V_{IL} = 0.8 V I_{OL} = 300 mA		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V, V_I = 0.4 V		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V, V_I = 5 V		8	11	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V, V_I = 0		56	76	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

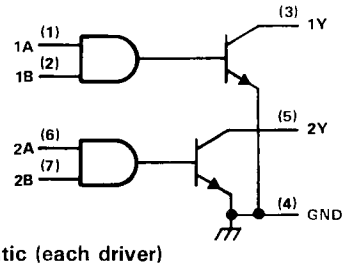
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 1		30	55	ns
t_{PHL}	Propagation delay time, high-to-low-level output			25	40	ns
t_{TLH}	Transition time, low-to-high-level output			8	20	ns
t_{THL}	Transition time, high-to-low-level output			10	20	ns
V_{OH}	High-level output voltage after switching	V_S = 55 V, $I_O \approx$ 300 mA, See Figure 2	V_S−18			mV

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

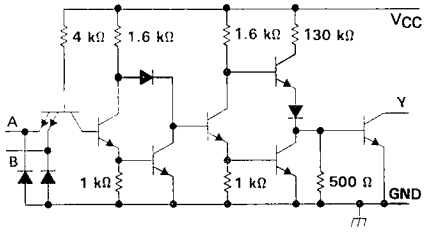


FUNCTION TABLE
(EACH DRIVER)

A	B	Y
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

positive logic
$Y = \overline{AB}$ or $\overline{A}+\overline{B}$

schematic (each driver)



Resistor values shown are nominal

electrical characteristics over recommended operating free-air temperature range

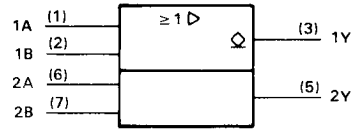
PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V, I_I = −12 mA		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{OH} = 70 V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.4	V
		V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 300 mA		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V, V_I = 0.4 V		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V, V_I = 5 V		13	17	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V, V_I = 0		61	76	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 1		45	65	ns
t_{PHL}	Propagation delay time, high-to-low-level output			30	50	ns
t_{TLH}	Transition time, low-to-high-level output			13	25	ns
t_{THL}	Transition time, high-to-low-level output			10	20	ns
V_{OH}	High-level output voltage after switching	V_S = 55 V, $I_O \approx$ 300 mA, See Figure 2	V_S−18			mV

logic symbol†



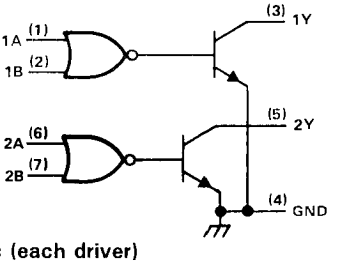
†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE
(EACH DRIVER)

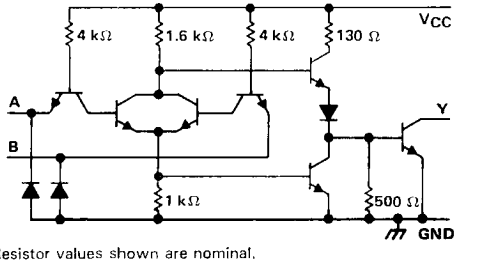
A	B	Y
L	L	L (on state)
L	H	H (off state)
H	L	H (off state)
H	H	H (off state)

positive logic:
$Y = A + B$ or $\overline{\overline{A}\,\overline{B}}$

logic diagram (positive logic)



schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

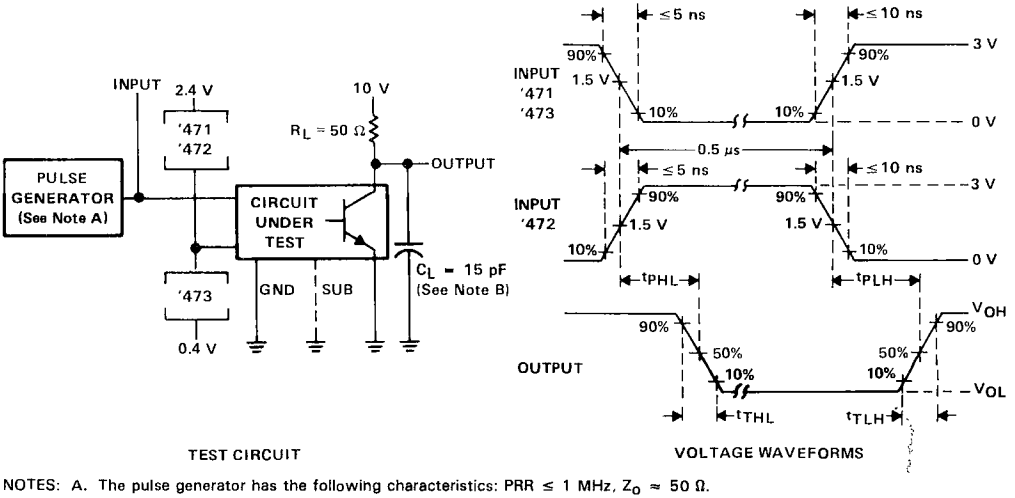
PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V, I_I = −12 mA		−1.2	−1.5	V
I_{OH}	High-level output current	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{OH} = 70 V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IL} = 0.8 V, I_{OL} = 100 mA		0.25	0.4	V
		V_{CC} = 4.75 V, V_{IL} = 0.8 V I_{OL} = 300 mA		0.5	0.7	
I_I	Input current at maximum input voltage	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V, V_I = 0.4 V		−1	−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V, V_I = 5 V		8	11	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V, V_I = 0		58	76	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	$I_O \approx$ 200 mA, C_L = 15 pF, R_L = 50 Ω, See Figure 1		30	55	ns
t_{PHL}	Propagation delay time, high-to-low-level output			25	40	ns
t_{TLH}	Transition time, low-to-high-level output			8	25	ns
t_{THL}	Transition time, high-to-low-level output			10	25	ns
I_{OH}	High-level output voltage after switching	V_S = 55 V, $I_O \approx$ 300 mA, See Figure 2	V_S−18			mV

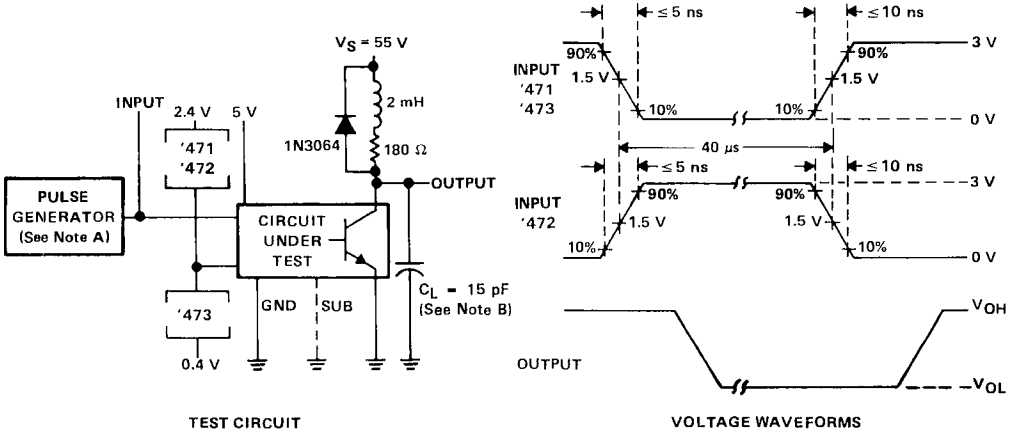
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, Z_O ≈ 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING TIMES



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR ≤ 12.5 kHz, Z_O ≈ 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 2. LATCH-UP TEST

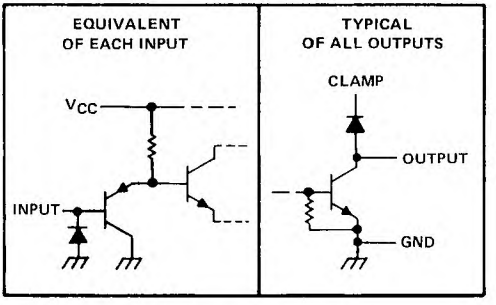
D2284, DECEMBER 1976—REVISED DECEMBER 1989

- Characterized for Use to 300 mA
- No Output Latch-Up at 55 V (After Conducting 300 mA)
- High-Voltage Outputs (100 V Typical)
- Output Clamp Diodes for Transient Suppression (300 mA, 70 V)
- TTL- or MOS-Compatible Diode-Clamped Inputs
- P-N-P Inputs Reduce Input Current
- Standard Supply Voltage
- Suitable for Hammer-Driver Applications
- Plastic DIP (P) with Copper Lead Frame Provides Cooler Operation and Improved Reliability

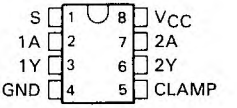
description

Series SN75476 dual peripheral drivers are designed for use in systems that require high current, high voltage, and fast switching times. The SN75476, SN75477, SN75478, and SN75479 provide AND, NAND, OR, and NOR drivers, respectively. These devices have diode-clamped inputs as well as high-current, high-voltage clamp diodes on the outputs for inductive transient protection.

The SN75476, SN75477, SN75478, and SN75479 drivers are characterized for operation from 0°C to 70°C.



D OR P PACKAGE
(TOP VIEW)



FUNCTION TABLES

SN75476
(EACH AND DRIVER)

INPUTS		OUTPUT
A	S	Y
H	H	H
L	X	L
X	L	L

SN75477
(EACH NAND DRIVER)

INPUTS		OUTPUT
A	S	Y
H	H	L
L	X	H
X	L	H

SN75478
(EACH OR DRIVER)

INPUTS		OUTPUT
A	S	Y
H	X	H
X	H	H
L	L	L

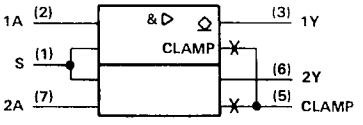
SN75479
(EACH NOR DRIVER)

INPUTS		OUTPUT
A	S	Y
H	X	L
X	H	L
L	L	H

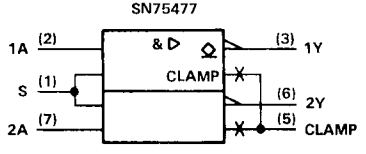
H = high level
L = low level
X = irrelevant

logic symbols†

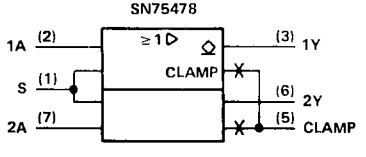
SN75476



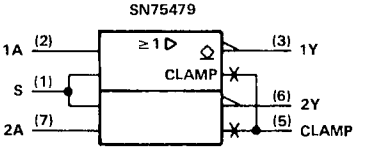
SN75477



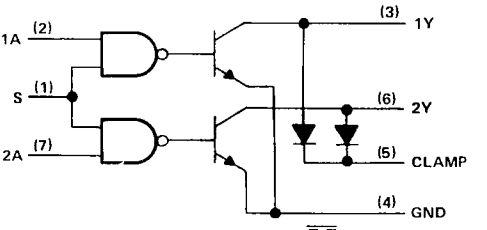
SN75478



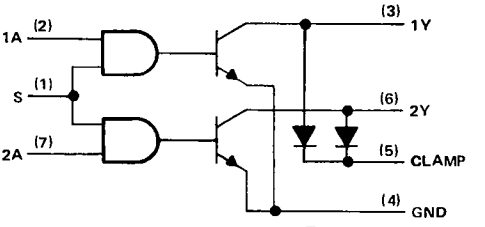
SN75479



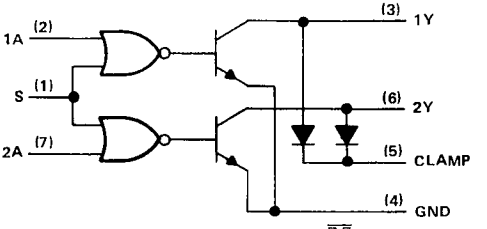
logic diagrams (positive logic)



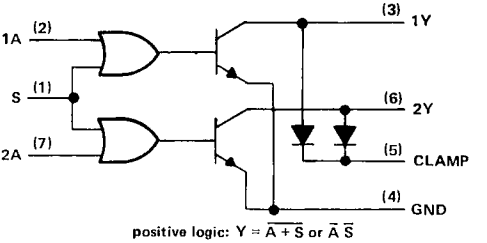
positive logic: $Y = AS$ or $\overline{\overline{A}+\overline{S}}$



positive logic: $Y = \overline{AS}$ or $\overline{A}+\overline{S}$



positive logic: $Y = A + S$ or $\overline{\overline{A}\,\overline{S}}$



positive logic: $Y = \overline{A+S}$ or $\overline{A}\,\overline{S}$

† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Continuous output current (see Note 2) . . . . . 400 mA
Peak output current: $t_W \leq 10$ ms, duty cycle $\leq 50\%$ . . . . . 500 mA
$t_W \leq 30$ ns, duty cycle $\leq 0.002\%$ . . . . . 3 A
Output clamp diode current . . . . . 400 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Both halves of this dual circuit may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation ratings.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range

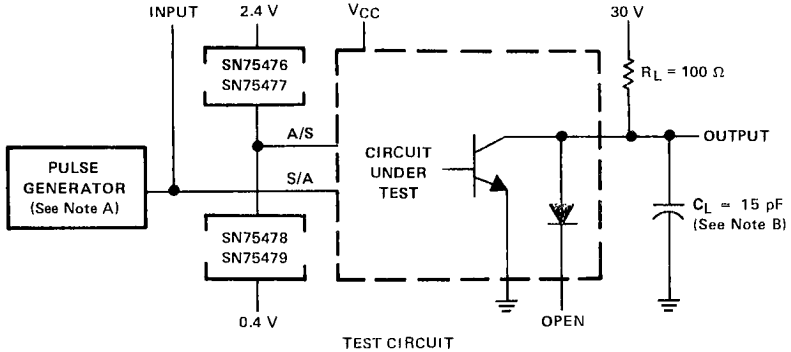
PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		$I_I = -12$ mA			−0.95	−1.5	V
I_{OH}	High-level output current		$V_{CC} = 4.5$ V, $V_{IL} = 0.8$ V,	$V_{IH} = 2$ V, $V_{OH} = 70$ V		1	100	μA
V_{OL}	Low-level output voltage		$V_{CC} = 4.5$ V, $V_{IH} = 2$ V, $V_{IL} = 0.8$ V	$I_{OL} = 100$ mA		0.16	0.3	V
				$I_{OL} = 175$ mA		0.22	0.5	
				$I_{OL} = 300$ mA		0.33	0.6	
$V_{(BR)O}$	Output breakdown voltage		$V_{CC} = 4.5$ V,	$I_{OH} = 100$ μA	70	100		V
$V_{R(K)}$	Output clamp diode reverse voltage		$V_{CC} = 4.5$ V,	$I_R =$ [illegible] μA	70	100		V
$V_{F(K)}$	Output clamp diode forward voltage		$V_{CC} = 4.5$ V,	$I_F =$ [illegible] mA	0.8	1.15	1.6	V
I_{IH}	High-level input current		$V_{CC} = 5.5$ V,	$V_I = 5.5$ V		0.01	10	μA
I_{IL}	Low-level input current	A input	$V_{CC} = 5.5$ V,	$V_I = 0.8$ V		−80	−110	μA
		Strobe S				−160	−220	
I_{CCH}	Supply current, outputs high	SN75476	$V_{CC} = 5.5$ V	$V_I = 5$ V		10	17	mA
		SN75477		$V_I = 0$		10	17	
		SN75478		$V_I = 5$ V		10	17	
		SN75479		$V_I = 0$		10	17	
I_{CCL}	Supply current, outputs low	SN75476	$V_{CC} = 5.5$ V	$V_I = 0$		54	75	mA
		SN75477		$V_I = 5$ V		54	75	
		SN75478		$V_I = 0$		54	75	
		SN75479		$V_I = 5$ V		54	75	

†All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

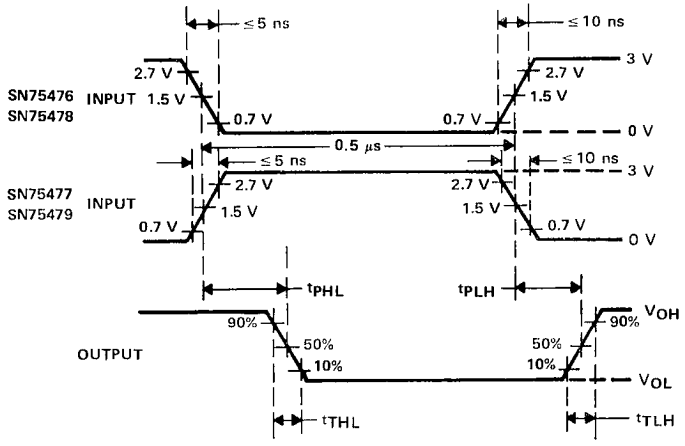
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 100 Ω, See Figure 1			ns
t_{PHL}	Propagation delay time, high-to-low-level output				ns
t_{TLH}	Transition time, low-to-high-level output				ns
t_{THL}	Transition time, high-to-low-level output		90		ns
V_{OH}	High-level output voltage after switching	V_S = 55 V, I_O ≈ 300 mA, See Figure 2	V_S − 18		mV

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

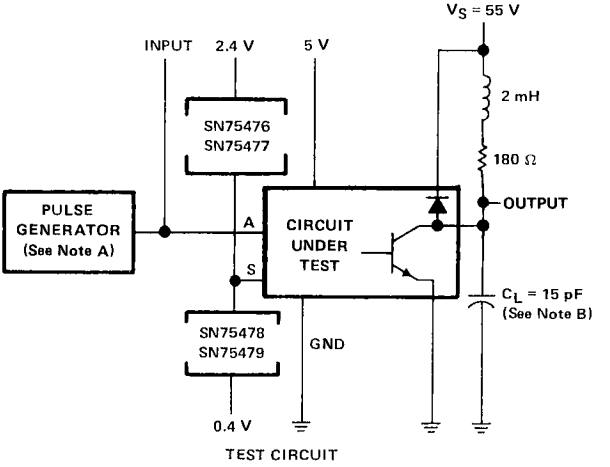


VOLTAGE WAVEFORMS

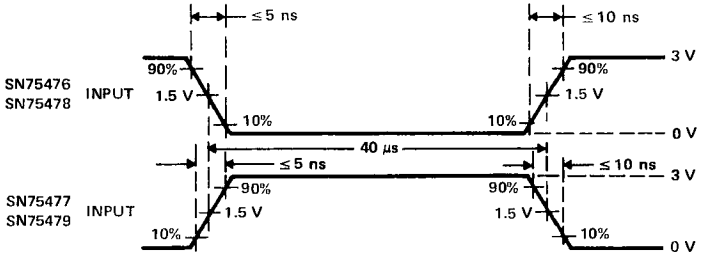
NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING CHARACTERISTICS

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

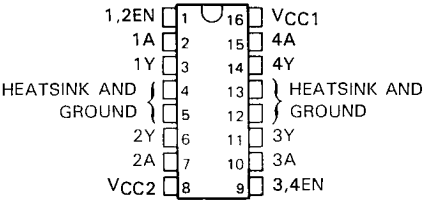
NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 2. LATCH-UP TEST

D2942, NOVEMBER 1986—REVISED MAY 1990

- 1-A Output Current Capability Per Driver
- Output Clamp Diodes for Inductive Transient Suppression
- Applications Include Half-H and Full-H Solenoid Drivers and Motor Drivers
- Designed for Positive-Supply Applications
- Wide Supply Voltage Range: 4.5 V to 36 V
- TTL- and CMOS-Compatible High-Impedance Diode-Clamped Inputs
- Separate Input-Logic Supply
- Thermal Shutdown
- Internal ESD Protection
- Input Hysteresis Improves Noise Immunity
- Three-State Outputs
- Minimized Power Dissipation
- Sink/Source Interlock Circuitry Prevents Simultaneous Conduction
- No Output "Glitch" During Power-Up or Power-Down
- Improved Functional Replacement for the SGS L293D

NE PACKAGE
(TOP VIEW)



FUNCTION TABLE
(EACH DRIVER)

INPUTS†		OUTPUT
A	EN	Y
H	H	H
L	H	L
X	L	Z

H = high-level
L = low-level
X = irrelevant
Z = high-impedance (off)
† In the thermal shutdown mode, the output is in high-impedance state regardless of the input levels.

description

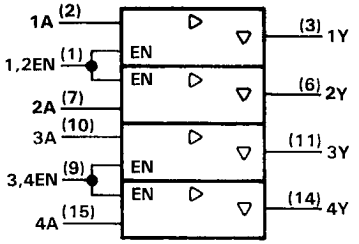
The SN754410 is a quadruple high-current half-H driver designed to provide bidirectional drive currents of up to one ampere at voltages from 4.5 V to 36 V. It is designed to drive inductive loads such as relays, solenoids, dc and bipolar stepping motors, as well as other high-current/high-voltage loads in positive-supply applications.

All inputs are compatible with TTL and low-level CMOS logic. Each output (Y) is a complete totem-pole driver with a Darlington transistor sink and a psuedo-Darlington source. Drivers are enabled in pairs with drivers 1 and 2 enabled by 1,2EN and drivers 3 and 4 enabled by 3,4EN. When an enable input is high, the associated drivers are enabled and their outputs become active and in phase with their inputs. When the enable input is low, those drivers are disabled and their outputs are off and in a high-impedance state. With the proper data inputs, each pair of drivers form a full-H (or bridge) reversible drive suitable for solenoid or motor applications.

A separate supply voltage (V_{CC1}) is provided for the logic input circuits to minimize device power dissipation. Supply voltage (V_{CC2}) is used for the output circuits.

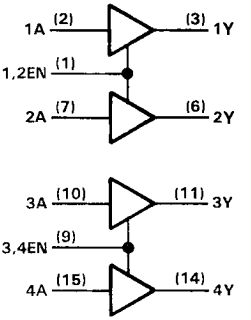
The SN754410 is designed for operation from −40°C to 85°C.

logic symbol†

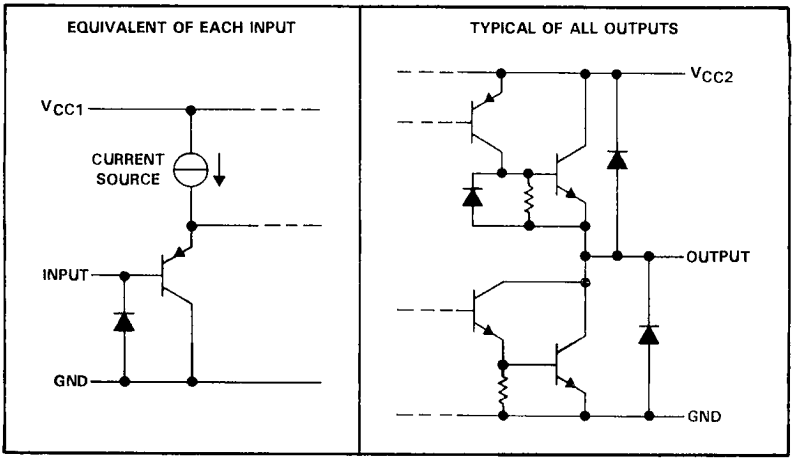


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and *IEC* Publication 617-12.

logic diagram



schematics of inputs and outputs



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Logic supply voltage range, V_{CC1} (see Note 1) . . . . . −0.5 V to 36 V
Output supply voltage range, V_{CC2} . . . . . −0.5 V to 36 V
Input voltage . . . . . 36 V
Output voltage range, V_O . . . . . −3 V to V_{CC2} + 3 V
Peak output current (nonrepetitive, $t_w \leq 5$ ms), I_{PK} . . . . . ±2 A
Continuous output current, I_O . . . . . ±1.1 A
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 2075 mW
Operating free-air temperature range . . . . . −40°C to 85°C
Operating case or virtual junction temperature range . . . . . −40°C to 150°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 16.6 mW/°C. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions

	MIN	MAX	UNIT
Logic supply voltage, V_{CC1}	4.5	5.5	V
Output supply voltage, V_{CC2}	4.5	36	V
High-level input voltage, V_{IH}	2	5.5	V
Low-level input voltage, V_{IL}	−0.3†	0.8	V
Operating virtual junction temperature, T_J	−40	125	°C
Operating free-air temperature, T_A	−40	85	°C

† The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet for logic voltage levels.

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, and operating virtual junction temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −12 mA			−0.9	−1.5	V
V_{OH}	High-level output voltage	I_{OH} = −0.5 A		V_{CC2}−1.5	V_{CC2}−1.1		V
		I_{OH} = −1 A		V_{CC2}−2			
		I_{OH} = −1 A, T_J = 25°C		V_{CC2}−1.8	V_{CC2}−1.4		
V_{OL}	Low-level output voltage	I_{OL} = 0.5 A			1	1.4	V
		I_{OL} = 1 A				2	
		I_{OL} = 1 A, T_J = 25°C			1.2	1.8	
V_{OKH}	High-level output clamp voltage	I_{OK} = 0.5 A			V_{CC2}+1.4	V_{CC2}+2	
		I_{OK} = 1 A			V_{CC2}+1.9	V_{CC2}+2.5	
V_{OKL}	Low-level output clamp voltage	I_{OK} = −0.5 A			−1.1	−2	V
		I_{OK} = −1 A			−1.3	−2.5	
I_{OZ}	Off-state (high-impedance state) output current	V_O = V_{CC2}					μA
		V_O = 0					
I_{IH}	High-level input current	V_I = 5.5 V					μA
I_{IL}	Low-level input current	V_I = 0				−10	μA
I_{CC1}	Logic supply current	I_O = 0	All outputs at high level			38	mA
			All outputs at low level			70	
			All outputs at high impedance			25	
I_{CC2}	Output supply current	I_O = 0	All outputs at high level			33	mA
			All outputs at low level			20	
			All outputs at high impedance			5	

†All typical values are at V_{CC1} = 5 V, V_{CC2} = 24 V, T_A = 25°C.

switching characteristics, V_{CC1} = 5 V, V_{CC2} = 24 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLH}	Delay time, low-to-high-level output from A input	C_L = 30 pF, See Figure 1		800		ns
t_{DHL}	Delay time, high-to-low-level output from A input			400		ns
t_{TLH}	Transition time, low-to-high-level output					ns
t_{THL}	Transition time, high-to-low-level output					ns
t_{PZH}	Enable time to the high level	C_L = 30 pF, See Figure 2				ns
t_{PZL}	Enable time to the low level					ns
t_{PHZ}	Disable time from the high level					ns
t_{PLZ}	Disable time from the low level			600		ns

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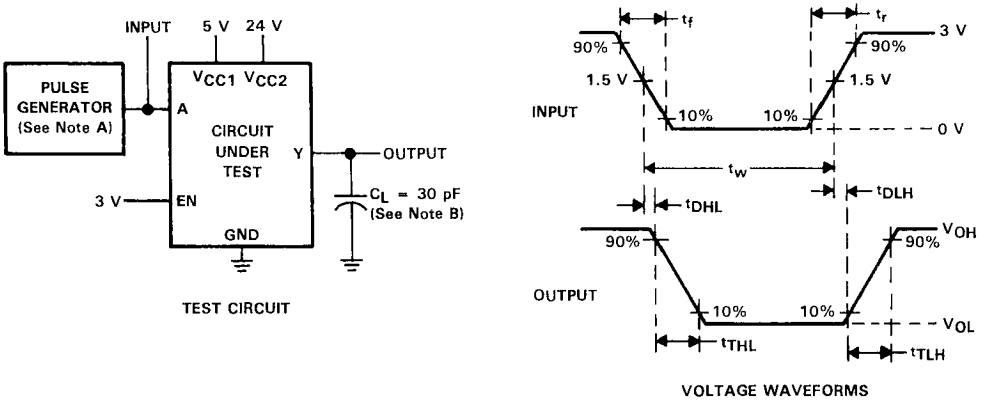
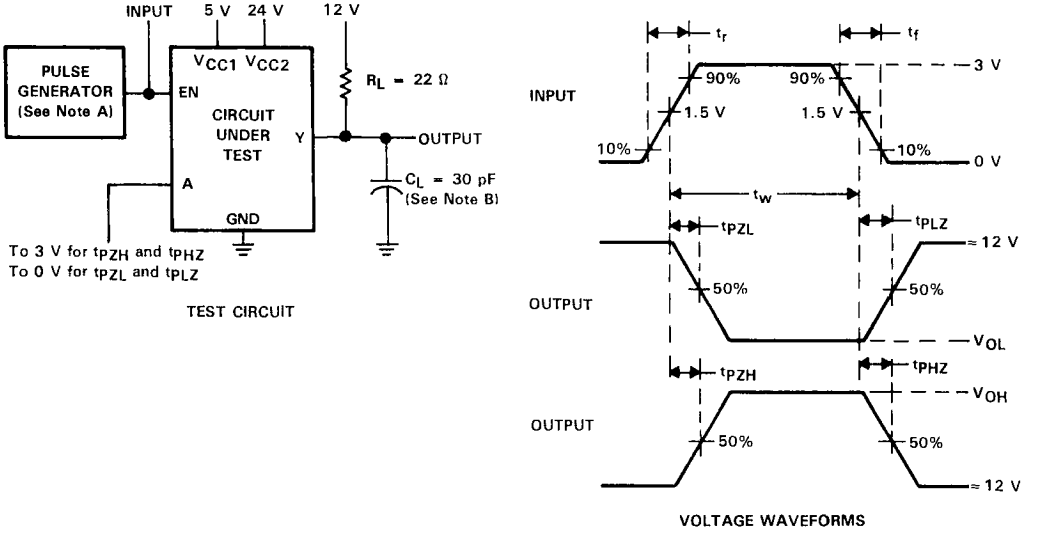
PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 10\ \mu s$, PRR = 5 kHz, $Z_o = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING TIMES FROM DATA INPUTS



NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 10\ \mu s$, PRR = 5 kHz, $Z_o = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 2. SWITCHING TIMES FROM ENABLE INPUTS

APPLICATION INFORMATION

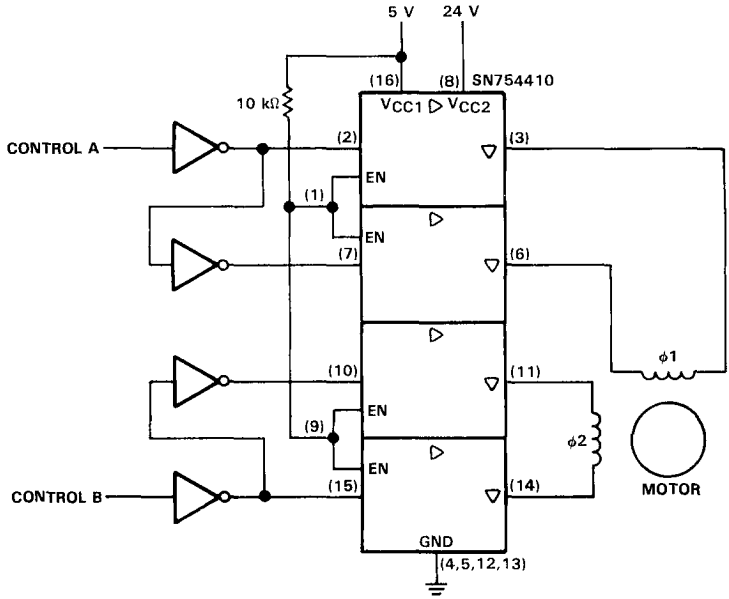


FIGURE 3. TWO-PHASE MOTOR DRIVER

TEXAS INSTRUMENTS
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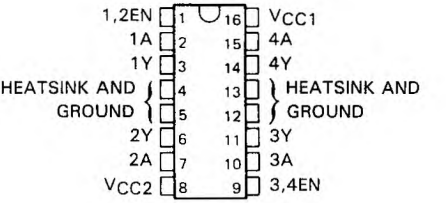
D2942, NOVEMBER 1986—REVISED MAY 1990

- 1-A Output Current Capability Per Driver
- Applications Include Half-H and Full-H Solenoid Drivers and Motor Drivers
- Designed for Positive-Supply Applications
- Wide Supply Voltage Range: 4.5 V to 36 V
- TTL- and CMOS-Compatible High-Impedance Diode-Clamped Inputs
- Separate Input-Logic Supply
- Thermal Shutdown
- Internal ESD Protection
- Input Hysteresis Improves Noise Immunity
- Three-State Outputs
- Minimized Power Dissipation
- Sink/Source Interlock Circuitry Prevents Simultaneous Conduction
- No Output "Glitch" During Power-Up or Power-Down
- Improved Functional Replacement for the SGS L293

NE PACKAGE
(TOP VIEW)



FUNCTION TABLE
(EACH DRIVER)

INPUTS†		OUTPUT
A	EN	Y
H	H	H
L	H	L
X	L	Z

H = high-level
L = low-level
X = irrelevant
Z = high-impedance (off)
† In the thermal shutdown mode, the output is in the high-impedance state regardless of the input levels.

description

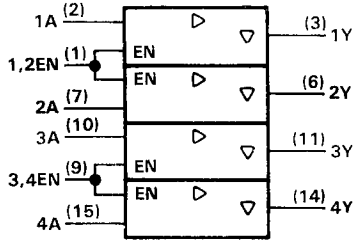
The SN754411 is a quadruple high-current half-H driver designed to provide bidirectional drive currents of up to one ampere at voltages from 4.5 V to 36 V. It is designed to drive inductive loads such as relays, solenoids, dc and bipolar stepping motors, as well as other high-current/high-voltage loads in positive-supply applications.

All inputs are compatible with TTL and low-level CMOS logic. Each output (Y) is a complete totem-pole driver with a Darlington transistor sink and a psuedo-Darlington source. Drivers are enabled in pairs with drivers 1 and 2 enabled by 1,2EN and drivers 3 and 4 enabled by 3,4EN. When an enable input is high, the associated drivers are enabled and their outputs become active and in phase with their inputs. When the enable input is low, those drivers are disabled and their outputs are off and in a high-impedance state. With the proper data inputs, each pair of drivers form a full-H (or bridge) reversible drive suitable for solenoid or motor applications.

External high-speed output clamp diodes should be used for inductive-transient suppression. A separate supply voltage (V_{CC1}) is provided for the logic input circuits to minimize device power dissipation. Supply voltage (V_{CC2}) is used for the output circuits.

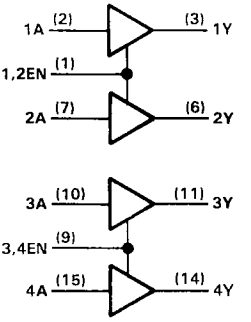
The SN754411 is designed for operation from −40°C to 85°C.

logic symbol†

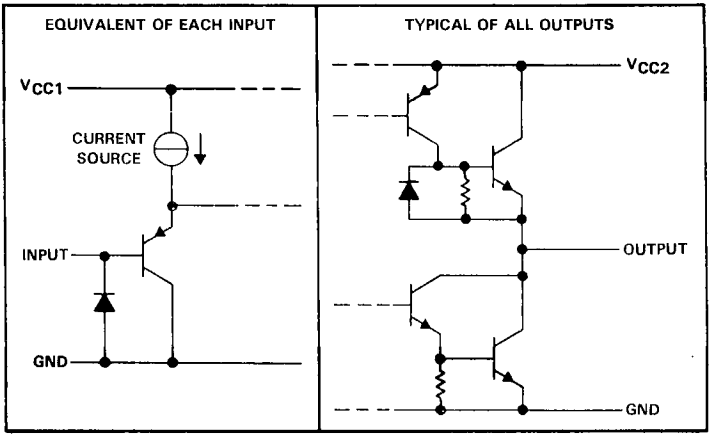


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Logic supply voltage range, V_{CC1} (see Note 1) . . . . . −0.5 V to 36 V
Output supply voltage range, V_{CC2} . . . . . −0.5 V to 36 V
Input voltage . . . . . 36 V
Output voltage range, V_O . . . . . −3 V to V_{CC2} + 3 V
Peak output current (nonrepetitive, $t_w \leq 5$ ms), I_{PK} . . . . . ±2 A
Continuous output current, I_O . . . . . ±1.1 A
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 2075 mW
Operating free-air temperature range . . . . . −40°C to 85°C
Operating case or virtual junction temperature range . . . . . −40°C to 150°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, derate linearly at the rate of 16.6 mW/°C. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions

	MIN	MAX	UNIT
Logic supply voltage, V_{CC1}	4.5	5.5	V
Output supply voltage, V_{CC2}	4.5	36	V
High-level input voltage, V_{IH}	2	5.5	V
Low-level input voltage, V_{IL}	−0.3†	0.8	V
Operating virtual junction temperature, T_J	−40	125	°C
Operating free-air temperature, T_A	−40	85	°C

† The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet for logic voltage levels.

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, and operating virtual junction temperature (unless otherwise noted)

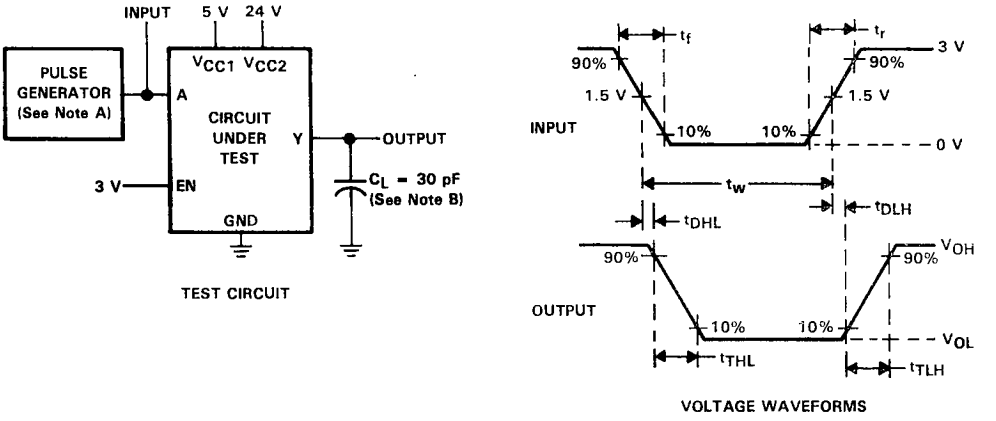
PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = −12 mA			−0.9	−1.5	V
V_{OH}	High-level output voltage	I_{OH} = −0.5 A		V_{CC2}−1.5	V_{CC2}−1.1		V
		I_{OH} = −1 A		V_{CC2}−2			
		I_{OH} = −1 A, T_J = 25°C		V_{CC2}−1.8	V_{CC2}−1.4		
V_{OL}	Low-level output voltage	I_{OL} = 0.5 A			1	1.4	V
		I_{OL} = 1 A				2	
		I_{OL} = 1 A, T_J = 25°C			1.2	1.8	
I_{OZ}	Off-state (high-impedance state) output current	V_O = V_{CC2}					μA
		V_O = 0					
I_{IH}	High-level input current	V_I = 5.5 V					μA
I_{IL}	Low-level input current	V_I = 0				−10	μA
I_{CC1}	Logic supply current	I_O = 0	All outputs at high level			38	mA
			All outputs at low level			70	
			All outputs at high impedance			25	
I_{CC2}	Output supply current	I_O = 0	All outputs at high level			33	mA
			All outputs at low level			20	
			All outputs at high impedance			5	

†All typical values are at V_{CC1} = 5 V, V_{CC2} = 24 V, T_A = 25°C.

switching characteristics, V_{CC1} = 5 V, V_{CC2} = 24 V, T_A = 25°C

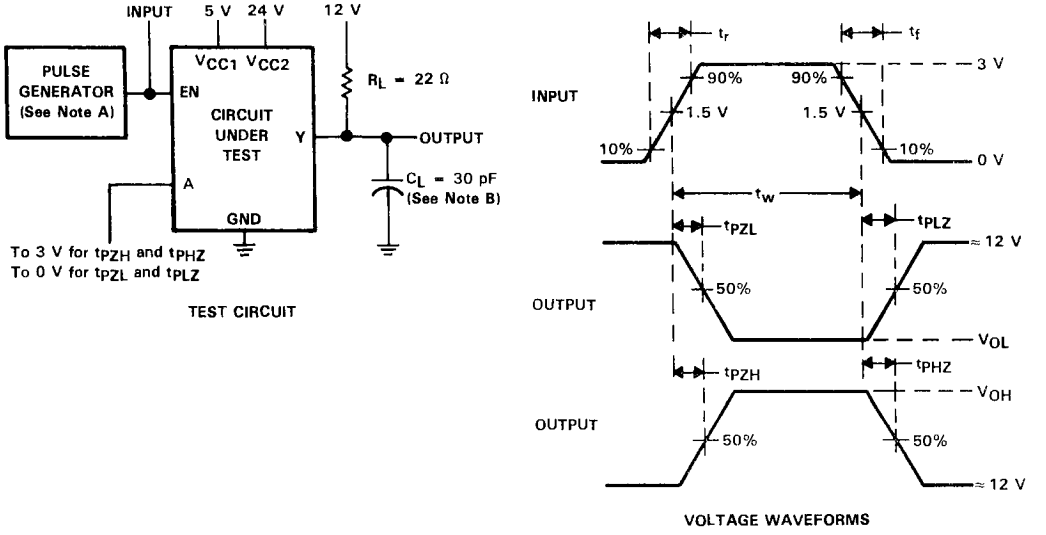
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLH}	Delay time, low-to-high-level output from A input	C_L = 30 pF, See Figure 1				ns
t_{DHL}	Delay time, high-to-low-level output from A input					ns
t_{TLH}	Transition time, low-to-high-level output			300		ns
t_{THL}	Transition time, high-to-low-level output					ns
t_{PZH}	Enable time to the high level	C_L = 30 pF, See Figure 2				ns
t_{PZL}	Enable time to the low level			400		ns
t_{PHZ}	Disable time from the high level			900		ns
t_{PLZ}	Disable time from the low level			600		ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Tha pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 10\ \mu s$, PRR = 5 kHz, $Z_o = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING TIMES FROM DATA INPUTS



NOTES: A. Tha pulse genarator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 10\ \mu s$, PRR = 5 kHz, $Z_o = 50\ \Omega$.
B. C_L includes probe and jig capacitanca.

FIGURE 2. SWITCHING TIMES FROM ENABLE INPUTS

APPLICATION INFORMATION

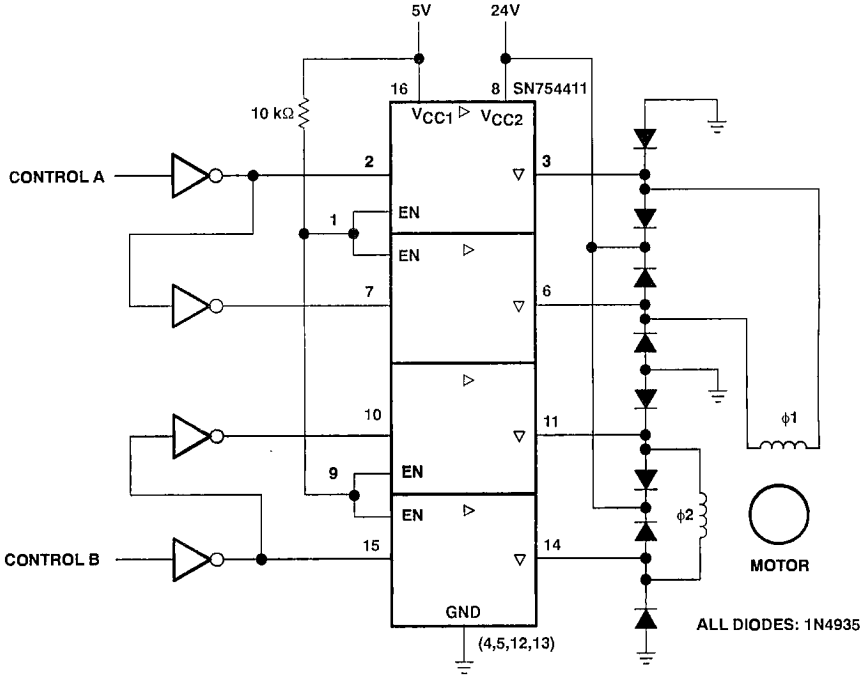
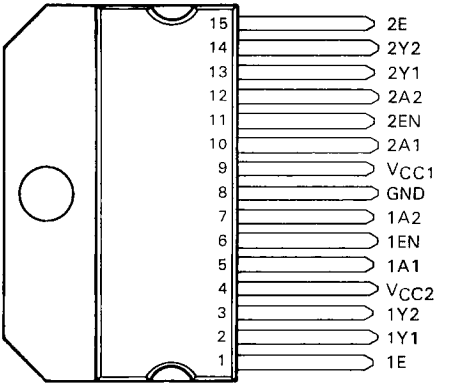


FIGURE 3. TWO-PHASE MOTOR DRIVER

D2942, JUNE 1987—REVISED JANUARY 1990

- Formerly TLP298
- 2-A Output Current Capability per Full-H Driver
- Applications Include Half-H and Full-H Solenoid Drivers and Motor Drivers
- Wide Range of Output Supply Voltage . . . 5 V to 46 V
- Separate Input-Logic Supply Voltage
- Thermal Shutdown
- Internal Electrostatic Discharge Protection
- High Noise Immunity
- Three-State Outputs
- Minimized Power Dissipation
- Sink/Source Interlock Circuitry Prevents Simultaneous Conduction
- Improved Functional Replacement for the SGS L298

KV PACKAGE
(TOP VIEW)



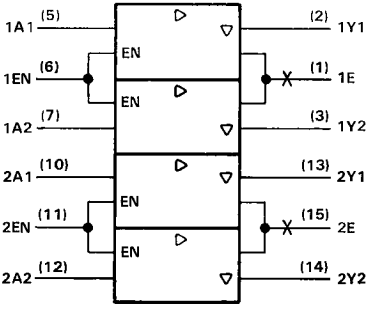
The tab is electrically connected to pin 8.

description

The TPIC0298 is a dual high-current full-H driver designed to provide bidirectional drive currents of up to two amperes at voltages from 5 V to 46 V. It is designed to drive inductive loads such as relays, solenoids, dc motors, stepping motors, and other high-current or high-voltage loads in positive-supply applications. All inputs are TTL compatible. Each output (Y) is a complete totem-pole drive with a Darlington transistor sink and a psuedo-Darlington source. Each full-H driver is enabled separately. Outputs 1Y1 and 1Y2 are enabled by 1EN and outputs 2Y1 and 2Y2 are enabled by 2EN. When an EN input is high, the associated channels are active. When an EN input is low, the associated channels are off (i.e., in the high-impedance state).

Each half of the device forms a full-H reversible driver suitable for solenoid or motor applications. The current in each full-H driver can be monitored by connecting a resistor between the sense output terminal 1E and ground and another resistor between sense output terminal 2E and ground.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE
(EACH CHANNEL)

INPUTS		OUTPUT
A	EN	Y
H	H	H
L	H	L
X	L	Z

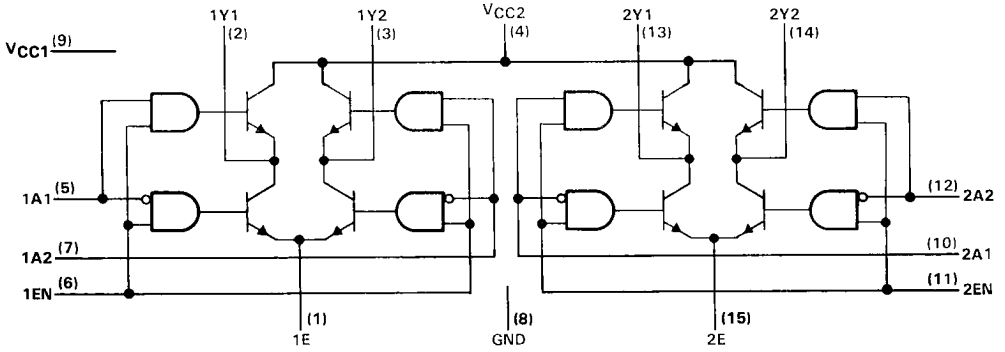
H = high-level
L = low-level
X = irrelevant
Z = high-impedance (off)

description (continued)

External high-speed output-clamp diodes should be used for inductive transient suppression. To minimize device power dissipation, a V_{CC1} supply voltage, separate from V_{CC2}, is provided for the logic inputs.

The TPIC0298 is designed for operation from 0°C to 70°C.

logic diagram (positive logic)



absolute maximum ratings over operating temperature range (unless otherwise noted)

Logic supply voltage range, V_{CC1}, (see Note 1) . . . . . −0.3 V to 7 V
Output supply voltage range, V_{CC2} . . . . . −0.3 V to 50 V
Input voltage range at A or EN, V_I (see Note 2) . . . . . −1.6 V to 7 V
Output voltage range, V_O . . . . . −2 V to V_{CC2}+2 V
Emitter terminal (1E and 2E) voltage range, V_E . . . . . −0.5 V to 2.3 V
Emitter terminal (1E and 2E) voltage (nonrepetitive, $t_w \leq 50\ \mu s$) . . . . . −1 V
Input current at A or EN, I_I . . . . . −15 mA
Peak output current, I_{OM}, (nonrepetitive, $t_w \leq 0.1$ ms) . . . . . ±3 A
(repetitive, $t_w \leq 10$ ms, duty cycle ≤ 80%) . . . . . ±2.5 A
Continuous output current, I_O . . . . . ±2 A
Peak combined output current for each full-H driver (see Note 3)
(nonrepetitive, $t_w \leq 0.1$ ms) . . . . . ±3 A
(repetitive, $t_w \leq 10$ ms, duty cycle ≤ 80%) . . . . . ±2.5 A
Continuous combined output current for each full-H driver (see Note 3) . . . . . ±2 A
Continuous dissipation at (or below) 25°C free-air temperature (see Note 4) . . . . . 3.575 W
Continuous dissipation at (or below) 75°C case temperature (see Note 4) . . . . . 25 W
Operating free-air, case, or virtual junction temperature range . . . . . −40°C to 150°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values are with respect to the network ground terminal, unless otherwise noted.
2. The maximum current limitation at this terminal generally occurs at a voltage of lower magnitude than the voltage limit, Neither the maximum current nor the maximum voltage for this terminal should be exceeded.
3. Combined output current applies to each of the two full-H drivers individually. This current is the sum of the currents at outputs 1Y1 and 1Y2 for full-H driver 1 and the sum of the currents at outputs 2Y1 and 2Y2 for full-H driver 2. The full-H drivers may carry the rated combined current simultaneously.
4. For operation above 25°C free-air temperature, derate linearly at the rate of 28.6 mW/°C. For operation above 75°C case temperature, derate linearly at the rate of 333 mW/°C. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipetion.

recommended operating conditions

		MIN	MAX	UNIT
Logic supply voltage, V_{CC1}		4.5	7	V
Output supply voltage, V_{CC2}		5	46	V
Emitter terminal (1E or 2E) voltage, V_E (see Note 5)		−0.5†	2	V
			$V_{CC1}-3.5$	
			$V_{CC2}-4$	
High-level input voltage, V_{IH} (see Note 5)	A	2.3	V_{CC1}	V
			$V_{CC2}-2.5$	
	EN	2.3	7	
			V_{CC1}	
Low-level input voltage at A or EN, V_{IL}		−0.3†	1.5	V
Output current, I_O			±2	A
Commutation frequency, f_c			40	kHz
Operating free-air temperature, T_A		0	70	°C

† The algebraic convention, in which the least positive (most negative) designated minimum, is used in this data sheet for emitter terminal voltage and logic voltage levels.

NOTE 5: For optimum device performance, the maximum recommended voltage at any A input is 2.5 V lower than V_{CC2}, the maximum recommended voltage at any EN input is V_{CC1}, and the maximum recommended voltage at any emitter terminal is 3.5 V lower than V_{CC1} and 4 V lower than V_{CC2}.

electrical characteristics over recommended ranges of V_{CC1}, V_{CC2}, and V_E, T_J = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = −12 mA				−0.9	−1.5	V
V_{OH}	High-level output voltage		I_{OH} = −1 A			V_{CC2}−1.8	V_{CC2}−1.2		V
			I_{OH} = −2 A			V_{CC2}−2.8	V_{CC2}−1.8		
V_{OL}	Low-level output voltage		I_{OL} = 1 A				V_E+1.2	V_E+1.8	V
			I_{OL} = 2 A				V_E+1.7	V_E+2.6	
V_{drop}	Total source plus sink output voltage drop		I_{OH} = −1 A, I_{OL} = 1 A	See Note 6			2.4	3.4	V
			I_{OH} = −2 A, I_{OL} = 2 A				3.5	5.2	
I_{OZH}	Off-state (high-impedance state) output current, high-level voltage applied		$V_O = V_{CC2}$					500	μA
I_{OZL}	Off-state (high-impedance state) output current, low-level voltage applied		V_O = 0 V, V_E = 0 V					−500	μA
I_{IH}	High-level input current	A	$V_I = V_{IH}$	EN = H			20	100	μA
				EN = L				10	
		EN	$V_I = V_{IH} \le V_{CC1}$−0.6 V				6	100	
I_{IL}	Low-level input current		V_I = 0 V to 1.5 V					−10*	μA
I_{CC1}	Logic supply current		I_O = 0	All outputs at high level			7	12	mA
				All outputs at low level			20	32	
				All outputs at high impedance			4	6	
I_{CC2}	Output supply current		I_O = 0	All outputs at high level			25	50	mA
				All outputs at low level			6	20	
				All outputs at high impedance				2	

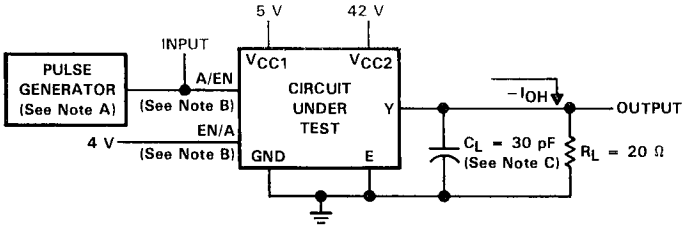
† All typical values are at V_{CC1} = 5 V, V_{CC2} = 42 V, V_E = 0 V, T_J = 25°C (unless otherwise noted).

NOTE 6: The V_{drop} specification applies for I_{OH} and I_{OL} applied simultaneously to different output channels.
$V_{drop} = V_{CC2} - V_{OH} + V_{OL} - V_E$.

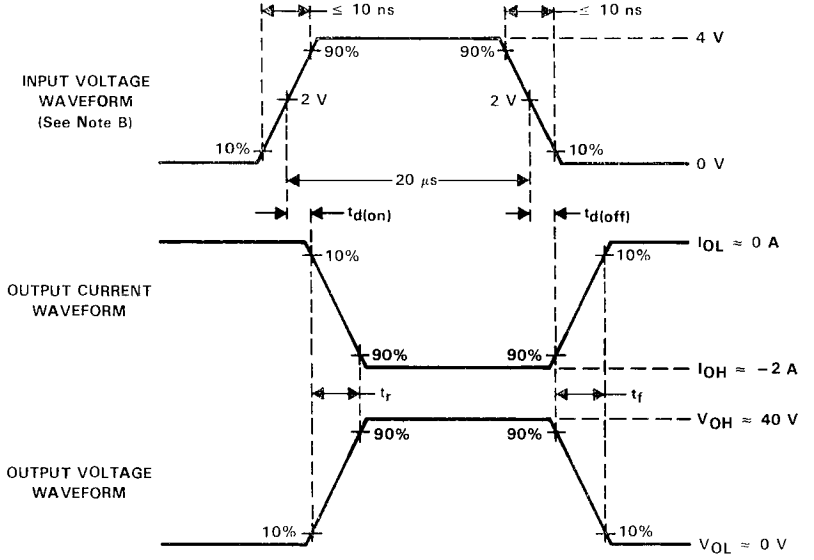
switching characteristics, V_{CC1} = 5 V, V_{CC2} = 42 V, V_E = 0, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Source current turn-on delay time from A input	C_L = 30 pF, See Figure 1		0.6		μs
$t_{d(off)}$	Source current turn-off delay time from A input			0.8		μs
t_r	Source current rise time (turning on)			0.8		μs
t_f	Source current fall time (turning off)			0.2		μs
$t_{d(on)}$	Source current turn-on delay time from EN input			0.5		μs
$t_{d(off)}$	Source current turn-off delay time from EN input			2.5		μs
$t_{d(on)}$	Sink current turn-on delay time from A input	C_L = 30 pF, See Figure 2		1.3		μs
$t_{d(off)}$	Sink current turn-off delay time from A input			0.5		μs
t_r	Sink current rise time (turning on)			0.2		μs
t_f	Sink current fall time (turning off)			0.2		μs
$t_{d(on)}$	Sink current turn-on delay time from EN input			0.3		μs
$t_{d(off)}$	Sink current turn-off delay time from EN input			1		μs

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

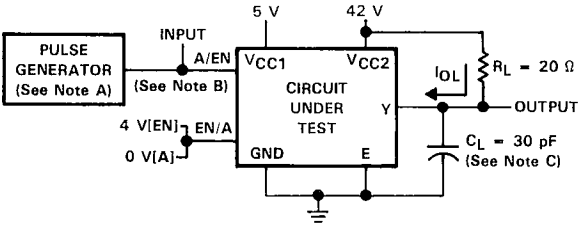


VOLTAGE AND CURRENT WAVEFORMS

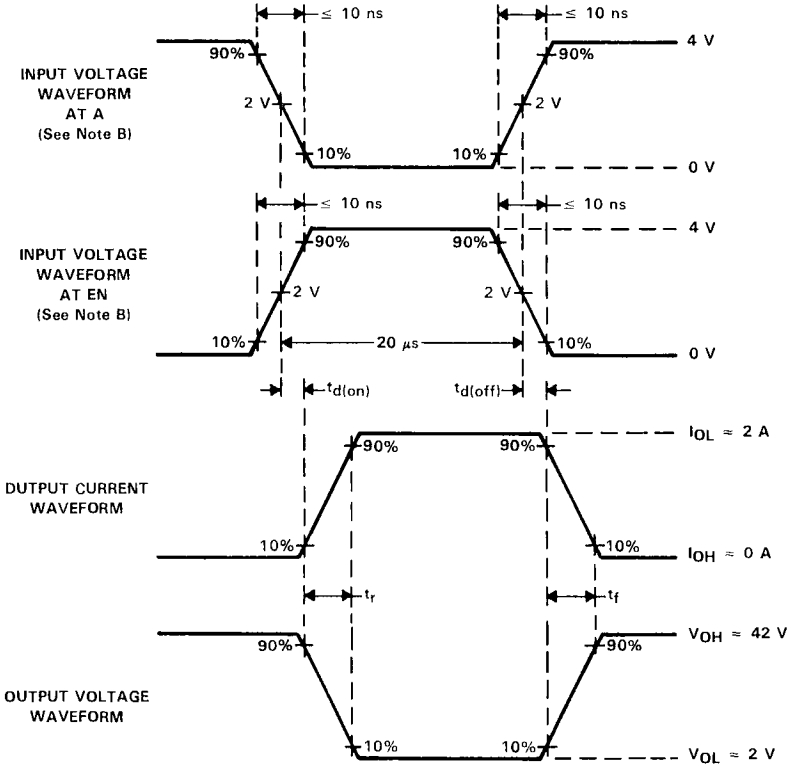
NOTES: A. The pulse generator has the following characteristics: PRR = 2 kHz, Z_O = 50 Ω.
B. EN is at 4 V if A is used as the switching input. A is at 4 V if EN is the switching input.
C. C_L includes probe and jig capacitance.

FIGURE 1. SOURCE CURRENT SWITCHING TIMES FROM DATA AND ENABLE INPUTS

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 2 kHz, Z_o = 50 Ω.
B. EN is at 4 V if A is used as the switching input. A is at 0 V if EN is the switching input.
C. C_L includes probe and jig capacitance.

FIGURE 2. SINK CURRENT SWITCHING TIMES FROM DATA AND ENABLE INPUTS

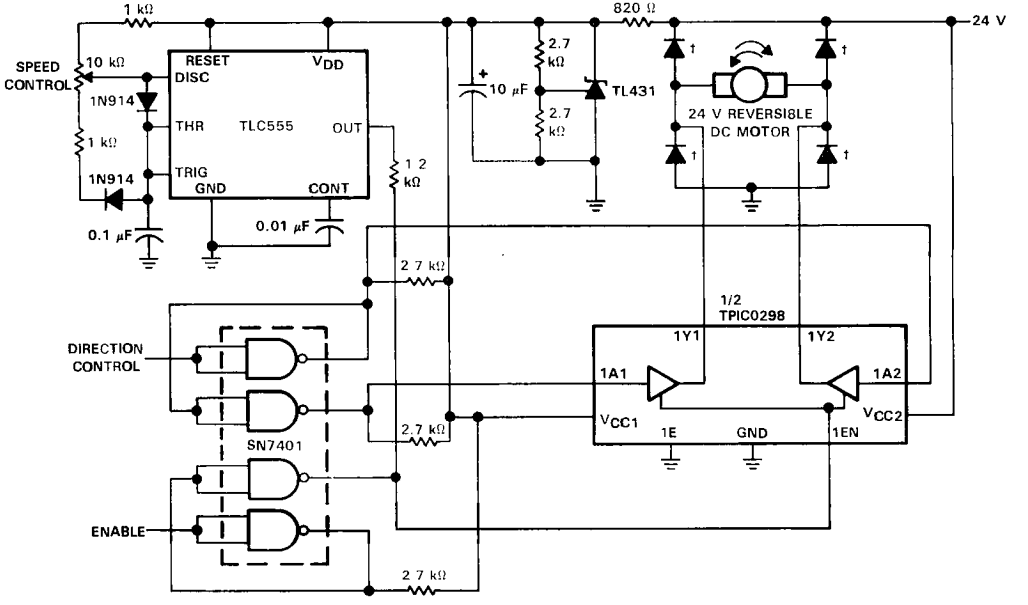
TYPICAL APPLICATION DATA

This circuit shows one half of a TPIC0298 used to provide full-H bridge drive for a 24-V 2-A dc motor. Speed control is achieved with a TLC555 timer. This provides variable duty cycle pulses to the EN input of the TPIC0298. In this configuration, the operating frequency is approximately 1.2 kHz. The duty cycle is adjustable from 10% to 90% to provide a wide range of motor speeds. The motor direction is determined by the logic level at the direction control input. The circuit may be enabled or disabled by the logic level at the EN input. A 5-V supply for the logic and timer circuit is provided by a TL431 short regulator. For circuit operation, refer to the function table.

FUNCTION TABLE

ENABLE	DIRECTION CONTROL	1Y1	1Y2
H	H	source	sink
H	L	sink	source
L	X	disabled	disabled

X = don't care H = high level L = low level



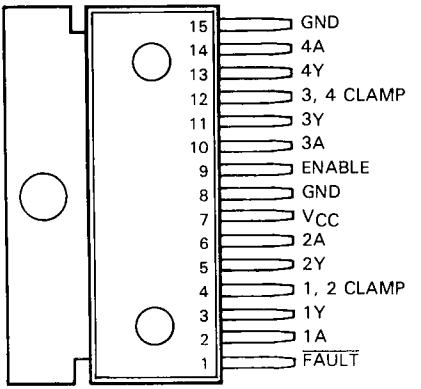
†Diodes are 1N4934 or equivalent.

FIGURE 3. TPIC0298 AS BIDIRECTIONAL DC MOTOR DRIVER

AUGUST 1989 – REVISED NOVEMBER 1989

- 1-A Current Capability Per Channel
- 45-V Inductive Switching Voltage Capability
- Current Sink Inputs Compatible with TTL or CMOS Devices
- Output Clamp Diodes for Inductive Transient Protection
- Independent Thermal Shutdown Protection
- Overvoltage Shutdown Protection
- Independent Channel Current Limit
- Error Sensing
- Extended Temperature Range of −40°C to 125°C

KN SINGLE-IN-LINE PACKAGE
(TOP VIEW)



The tab is electrically connected to the GND pins.

description

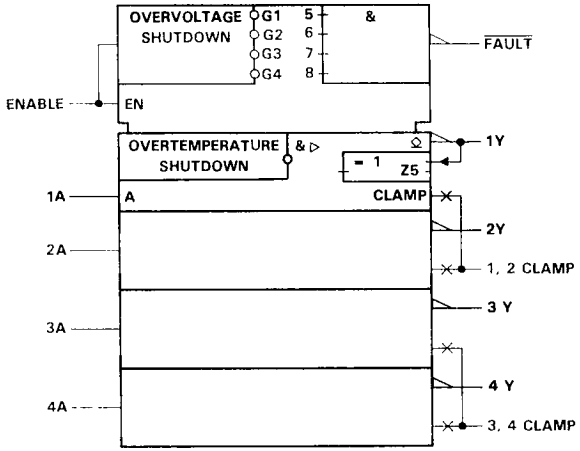
The TPIC2404 is a monolithic high-voltage high-current quadruple low-side switch especially designed for driving from low-level logic to peripheral loads such as relays, solenoids, motors, lamps, and other high-voltage high-current loads. The high-efficiency power switch is optimized for applications where a very rugged power switch is required. The device will tolerate power supply transients and reverse battery conditions up to 13 V.

The TPIC2404 features four inverting open-collector outputs controlled by a common-enable input. When ENABLE is low, the c . · .ts are disabled. An error sensing circuit monitors load and device faults. When an error is sensed, the ∴ $\overline{FLT}$ output goes to a low state. In addition, the device features on-board V_{CC} overvoltage and thermal overload protection circuits, and the outputs are current-limit protected.

FUNCTION TABLE

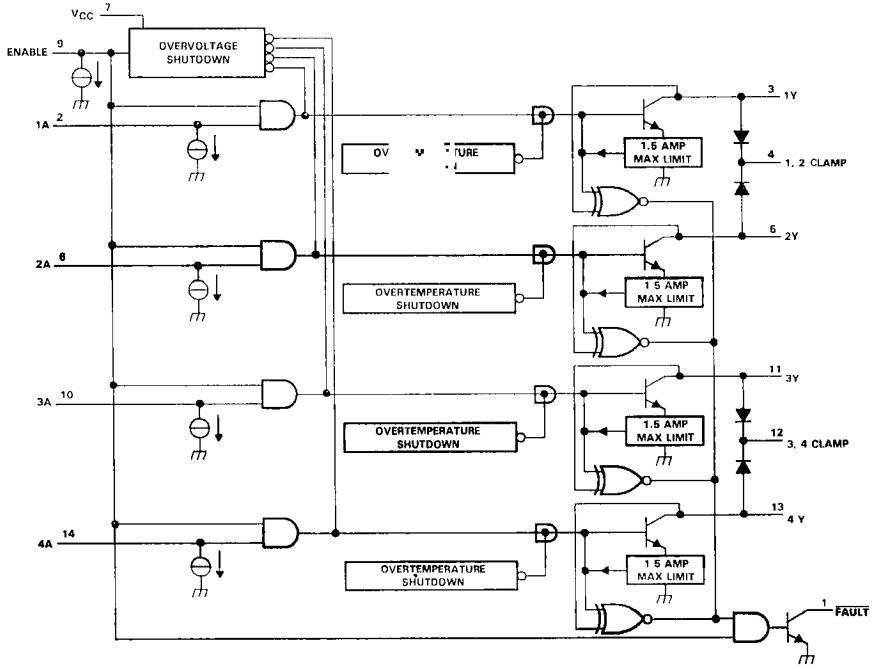
	ENABLE	A	Y	$\overline{FAULT}$
Normal operation	H H L	H L X	L H H	H H H
Open load	H	L	L	L
Short to GND				
Overvoltage shutdown	H	X	H	L
Thermal shutdown				
Short to V_{CC}	H	H	H	L

logic symbol†

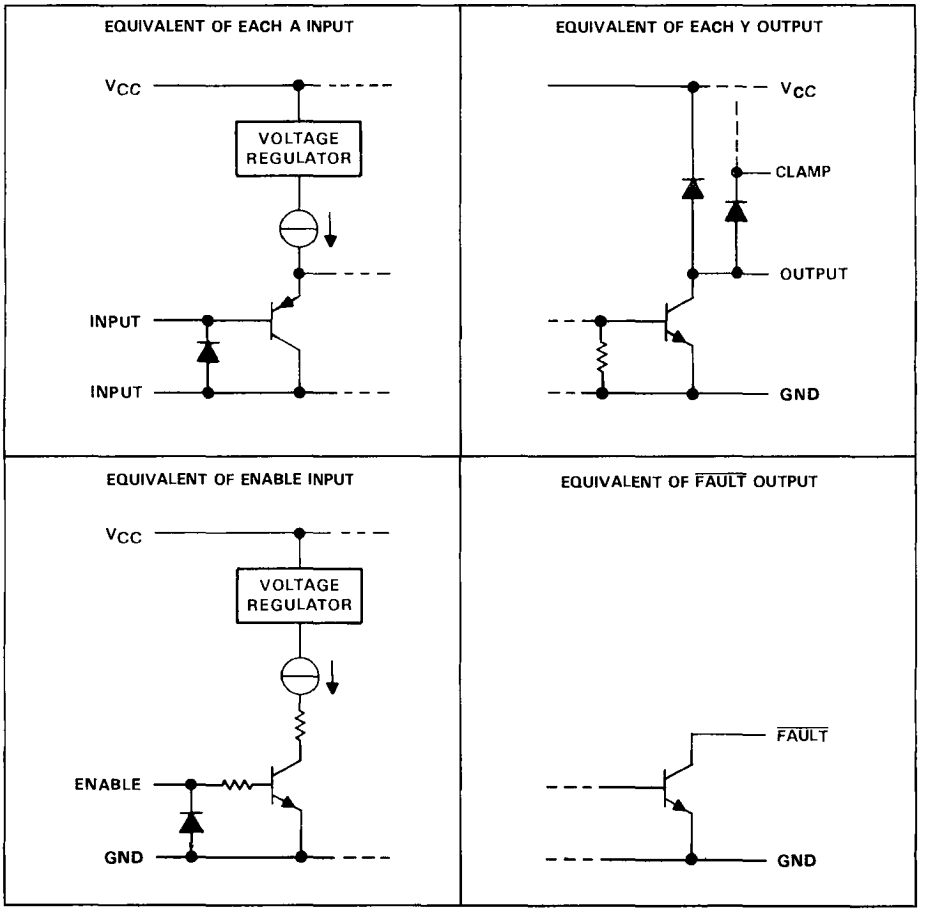


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) . . . . . −13 V to 24 V
Input voltage range, V_I . . . . . −0.6 V to 7 V
Output voltage range, V_O . . . . . −0.6 V to 45 V
Output sustaining voltage, $V_{O(sust)}$ . . . . . 45 V
Continuous output sink current (repetitive, t_w < 8 ms), I_{OL} (see Note 2) . . . . . 1.5 A
Output clamp-diode voltage, V_{OK} . . . . . 45 V
Continuous total dissipation at (or below) 25°C case temperature (see Note 3) . . . . . 50 W
Operating case or virtual junction temperature range . . . . . −55°C to 150°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 s . . . . . 260°C

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. Output sink current is limited by the overcurrent limit.
3. For operation above 25°C free-air or case temperature refer to Figures 1 and 2. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below rated dissipation.

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

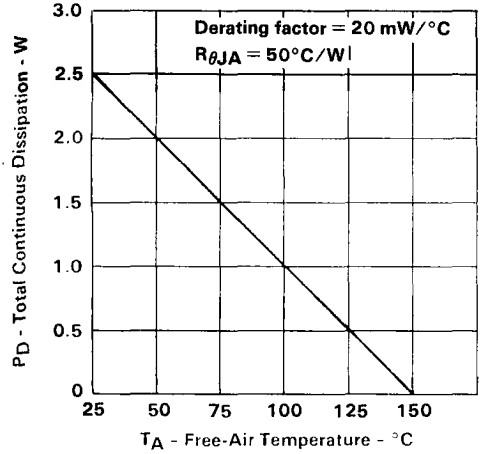


FIGURE 1

CASE TEMPERATURE
DISSIPATION DERATING CURVE

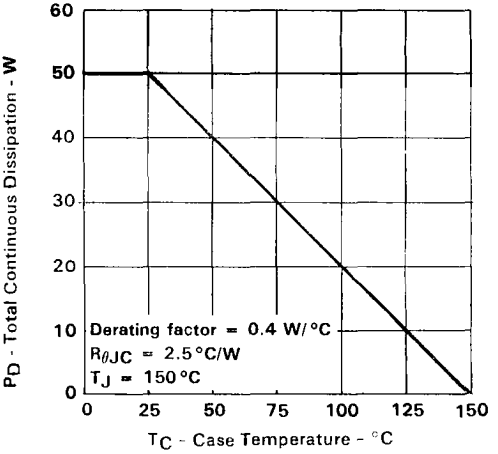


FIGURE 2

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	9	12	16	V
High-level input voltage, V_{IH}	2		5.5	V
Low-level input voltage, V_{IL}	−0.3†		0.8	V
Peak output voltage from external inductive kickback			45	V
Continuous output sink current			1	A
Fault output sink current			75	μA
Operating free-air temperature, T_A	−40		125	°C

† The algebraic convention in which the least positive (most negative) value is designated minimum is used in this data sheet for logic voltage levels.

electrical characteristics over recommended ranges of operating free-air temperature and supply voltages (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
$I_{O(off)}$	Off-state output current		V_O = 12 V, ENABLE low		15	100	μA
			V_O = 45 V, ENABLE high		0.6	2	mA
			V_O = 12 V, ENABLE high	200	400	600	μA
I_{IL}	Low-level input current		V_I = 0 to 0.8 V	−10	25	40	μA
I_{IH}	High-level input current	A inputs		10	25	60	μA
		ENABLE			0.2	1	mA
V_{OL}	Low-level output voltage		I_{OL} = 100 mA		0.1	0.15	V
			I_{OL} = 500 mA		0.3	0.55	
			I_{OL} = 1 A		0.8	1.3	
			$\overline{FAULT}$ output, I_{OL} = 30 μA		0.2	0.4	
I_{OL}	Low-level output current		$\overline{FAULT}$ output, V_{OL} = 1 V to 5.5 V	50	90	125	μA
$I_{R(K)}$	Clamp diode reverse current		V_r = 50 V, V_O = 0			100	μA
$V_{F(K)}$	Clamp diode forward voltage		I_f = 1 A			2	V
			I_f = 1.5 A			2.5	
I_{CC}	Supply current		Outputs off, ENABLE low			0.25	mA
			Outputs on, T_A = −40°C			120	
			Outputs on, T_A = 25° C to 125°C			100	

operating characteristics over recommended operating free-air temperature and supply voltages (unless otherwise noted)

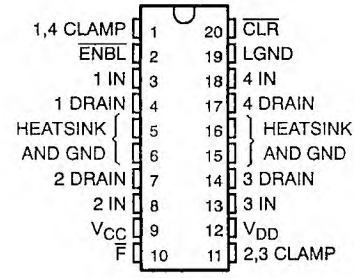
PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
High-level				7	V
Low-level		3			V
Overcurrent limiting	T_A = −40°C			1.85	A
	T_A = 25°C to 125°C		1.2	1.5	
V_{CC} Overv[illegible] shutdown		25.5		31	V
V_{hys} Ove[illegible]ges shutdown hysteresis			[illegible]		V
Thermal shutdown			1[illegible]		°C
Thermal shutdown hysteresis			15		°C
Turn-on time			8		μs
Turn-off time			8		μs

‡ All typical values are at V_{CC} = 12 V, T_A = 25 °C.

D3378, FEBRUARY 1990

- **Output Voltage up to 60 V**
- **4 Output Channels of 700-mA Nominal Current Per Channel**
- **Pulsed Current 3 A Per Channel**
- **Low $r_{DS(on)}$ . . . 0.5 Ω Typ**
- **Avalanche Energy . . . 50 mJ**
- **Thermal Shutdown Protection with Fault (Overtemperature) Output**
- **NE Package Designed for Heat Sinking**
- **Integral Output Clamp Diodes**
- **Input Transparent Latches for Data Storage**
- **Asynchronous Clear to Turn Off All Outputs**
- **Output Parallel Capability for Increased Current Drive up to 12-A Total Pulsed Load Current**

NE PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each channel)

FUNCTION	INPUTS			OUTPUT	FAULT
	ENBL	CLR	IN	Y	F
NORMAL OPERATION	^	L	X	H	H
	L	H	L	H	H
	L	H	H	L	H
	H	H	X	Q_0	H
THERMAL SHUTDOWN	X	X	X	H	L

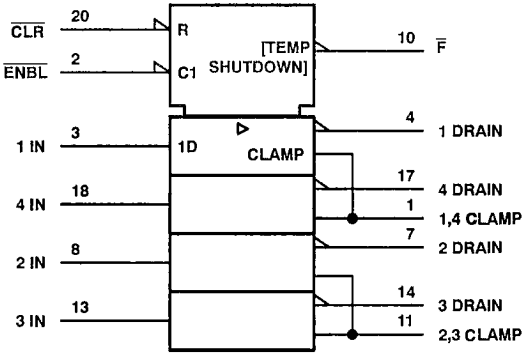
H = high-level, L = low-level, X = irrelevant

description

The TPIC2406 is a monolithic, high-voltage, high-current, quadruple power driver designed for use in systems that require high load power. The device contains built-in high-speed output clamp diodes for inductive transient protection. Power driver applications include lamps, relays, solenoids, and dc stepping motors.

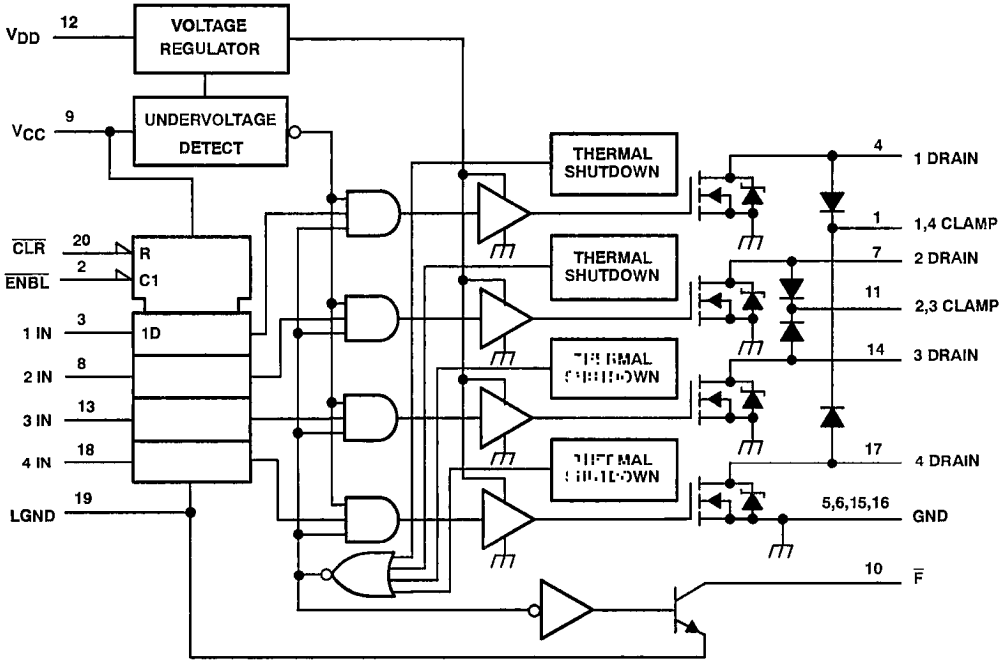
Each device features four inverting open-drain outputs each controlled by an input storage latch with common clear and enable controls. All inputs accept standard TTL- and CMOS-level signals. The $\overline{CLR}$ function is asynchronous and turns all four outputs off regardless of data inputs. Taking $\overline{ENBL}$ low puts the input latch into a transparent mode, allowing the data inputs to affect the output. In this state, all four outputs will be held off while $\overline{CLR}$ is low, but will return to the stages on the data inputs when $\overline{CLR}$ goes high. When $\overline{ENBL}$ is taken high, the latch is put into a storage mode and the last state of the data inputs is held in the latches. If the $\overline{CLR}$ input is taken low, the data in the latches is cleared, turning all outputs off. If $\overline{CLR}$ is taken high again, $\overline{ENBL}$ must be cycled low to read new data into the latch.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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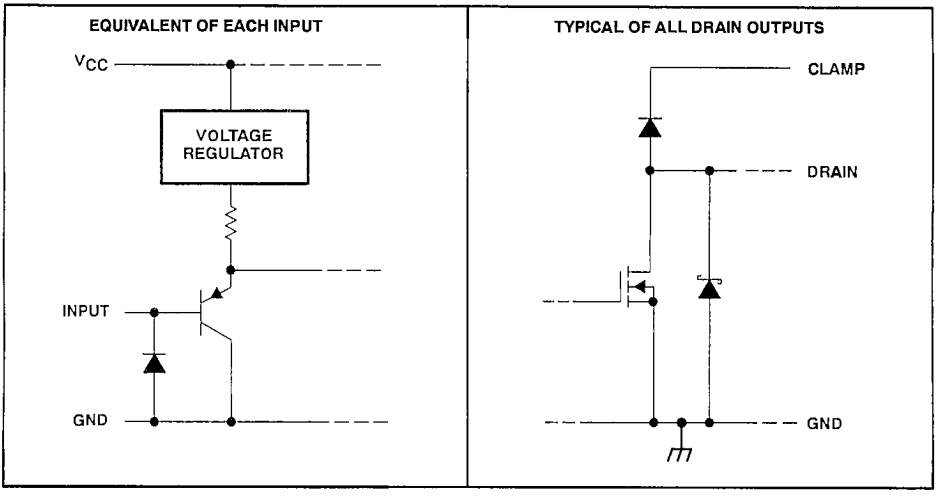
schematics of inputs and outputs



absolute maximum ratings over – 40°C to 125°C case temperature range (unless otherwise noted)

Logic supply voltage, V_{CC} (see Note 1)	7 V
Power MOSFET driver supply voltage, V_{DD}	60 V
Logic input voltage, V_I	7 V
Power MOSFET drain-source voltage, V_{DS}	60 V
$\overline{F}$ output voltage	7 V
Clamp diode voltage	60 V
Continuous source-drain diode anode current	1.25 A
Pulsed source-drain diode anode current	6 A
Pulsed drain current, each output, all outputs on; $I_{D1} = I_{D2} = I_{D3} = I_{D4}$, T_A = 25°C (see Note 2 and Figures 5 through 8)	3 A
Continuous drain current, each output, all outputs on, $I_{D1} = I_{D2} = I_{D3} = I_{D4}$, T_A = 25°C	770 mA
Peak drain current, single output, I_{DM}, T_A = 25°C (see Note 3)	12.5 A
Single-pulse avalanche energy, E_{AS}	50 mJ
Continuous total dissipation at or below 25°C free-air temperature (see Note 4)	2.5 W
Continuous total dissipation at or below 100°C case temperature (see Note 4)	6 W
Operating junction temperature range, T_J	– 40°C to 150°C
Storage temperature range	– 40°C to 150°C
Lead temperature	260°C

NOTES: 1. All voltage values are with respect to the five ground (GND and LGND) terminals connected together.
2. Pulse duration = 10 ms, duty cycle = 6%.
3. Pulse duration ≤ 100 μs, duty cycle ≤ 2%.
4. For operation above 25°C free-air temperature, derate linearly at the rate of 20 mW/°C. For operation above 100°C case temperature, derate linearly at the rate of 120 mW/°C. To avoid exceeding the design maximum junction temperature, these ratings should not be exceeded. Due to variations in individual devices, electrical characteristics, and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Logic supply voltage, V_{CC}		4.5		5.5	V
Output supply voltage, V_{DD}		10		35	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.6	V
Setup time, t_{su}, data before $\overline{ENBL}$ ↑ (see Figure 1)		100			ns
Hold time, t_h, data after $\overline{ENBL}$ ↑ (see Figure 1)		100			ns
Pulse duration, t_w (see Figure 1)	$\overline{ENBL}$ low	300			ns
	$\overline{CLR}$ low				
Operating case temperature, T_C		−40		125	°C

electrical characteristics, V_{CC} = 5 V, V_{DD} = 14 V, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-source breakdown voltage	I_D = 1 mA		60			V
$V_{F(K)}$	Clamp diode forward voltage	I_F = 1.25 A,	See Notes 5 and 6			1.6	V
V_{SD}	Source-drain diode forward voltage	I_S = 1.25 A,	See Notes 5 and 6			1.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5	V
V_{OL}	$\overline{F}$ low-level output voltage	I_{OL} = 4 mA			0.4		V
I_{IH}	High-level input current	V_{CC} = 5.5 V,	V_I = 2.7 V			20	µA
I_{IL}	Low-level input current	V_{CC} = 5.5 V,	V_I = 0.4 V			0.1	mA
I_{CC}	Logic supply current	I_O = 0,	All outputs off			10	mA
I_N	Nominal current	$V_{DS(on)}$ = 0.5 V, T_C = 85°C,	$I_N = I_D$, See Notes 5, 6, and 7		700		mA
I_{DD}	Output supply current	I_O = 0,	All outputs off			6	mA
$I_{R(K)}$	Clamp-diode reverse current	V_{DS} = 55 V,	V_O = 0			1	µA
		V_{DS} = 55 V,	V_O = 0, T_C = 125°C			10	
I_{DSX}	Off-state drain current	V_R = 55 V,				1	µA
		V_R = 55 V,	T_C = 125°C			10	
$I_{O(\overline{F})}$	High-level fault leakage current	V_{OH} = 5.5 V				1	µA
$r_{DS(on)}$	Static drain-source on-state resistance	I_D = 1.25 A	See Notes 5 and 6		0.5	0.6	Ω
		I_D = 1.25 A, T_C = 125°C			0.8	1	
		I_D = 3 A			0.55	0.65	

NOTES: 5. Technique should limit $T_j - T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
7. Nominal current is defined for a consistent comparison between devices from different sources. It is the current that produces a voltage drop of 0.5 V at 85°C at case temperature.

switching characteristics, V_{CC} = 5 V, V_{DD} = 24 V, T_C = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level drain output from clock	C_L = 30 pF,	See Figure 1		450		ns
t_{PHL}	Propagation delay time, high-to-low-level drain output from clock				550		ns
t_{TLH}	Transition time, low-to-high-level of source-drain output				35		ns
t_{THL}	Transition time, high-to-low-level of source-drain output				30		ns
t_{DLH}	Delay time, low-to-high-level drain output from input	C_L = 30 pF, I_D = I_N = 700 mA	See Figure 2,		380		ns
t_{DHL}	Delay time, high-to-low-level drain output from input				380		ns
t_{RLH}	Rise time, low-to-high-level of source-drain output				35		ns
t_{FHL}	Fall time, high-to-low-level of source-drain output				70		ns
t_a	Reverse-recovery-current rise time	I_F = 3 A, See Notes 5 and 6,	di/dt = 100 A/µs, See Figure 3		45		ns

NOTES: 5. Technique should limit $T_j - T_C$ to 10°C maximum.
6. These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

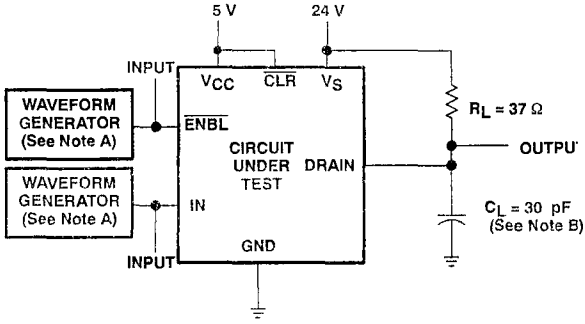
thermal resistance

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance	All four outputs with equal power			8.33	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance				50	°C/W

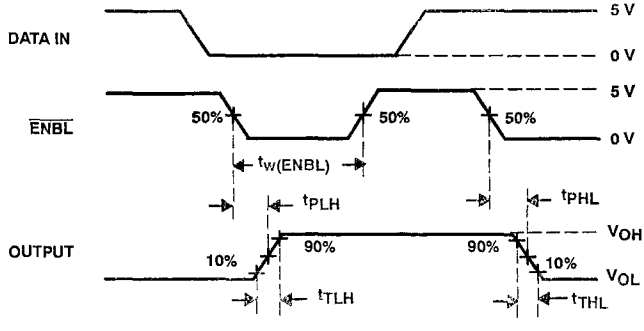
operating characteristics over – 40°C to 125°C case temperature range

PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Undervoltage shutdown	3		4.5	V
	Thermal shutdown temperature		155		°C
	Thermal shutdown hysteresis		15		°C

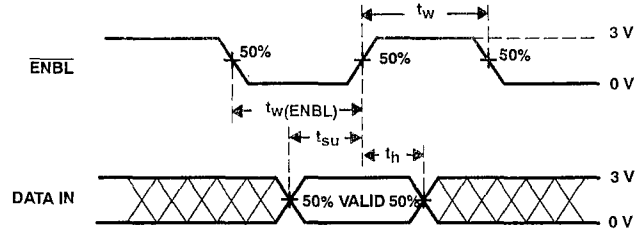
PARAMETER MEASUREMENT INFORMATION



(a) TEST CIRCUIT



(b) SWITCHING TIMES FROM ENABLE INPUT



(c) INPUT SETUP AND HOLD WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 300$ ns, PRR = 5 kHz, $Z_o = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1. SWITCHING TIMES

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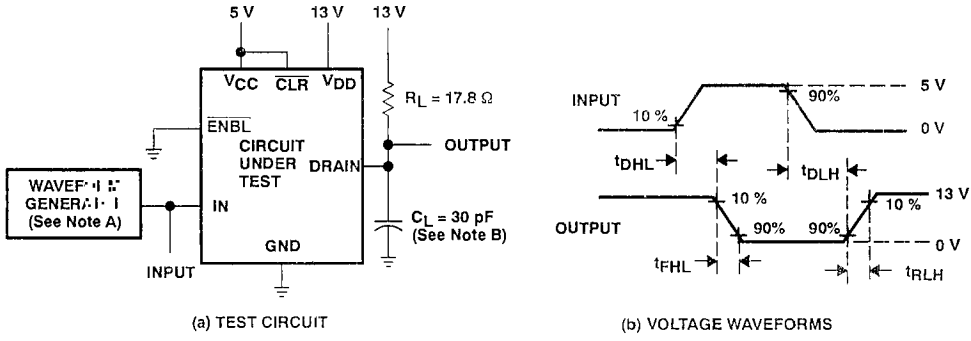
PARAMETER MEASUREMENT INFORMATION



(a) TEST CIRCUIT

(b) VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \le 10$ ns, $t_f \le 10$ ns, $t_w = 5$ ms, PRR = 5 kHz, $Z_O = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 2. SWITCHING TIMES

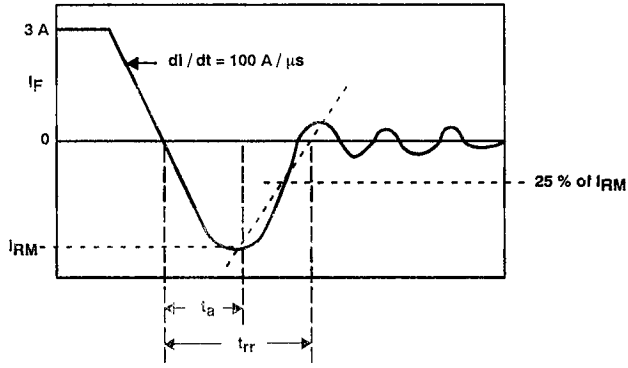
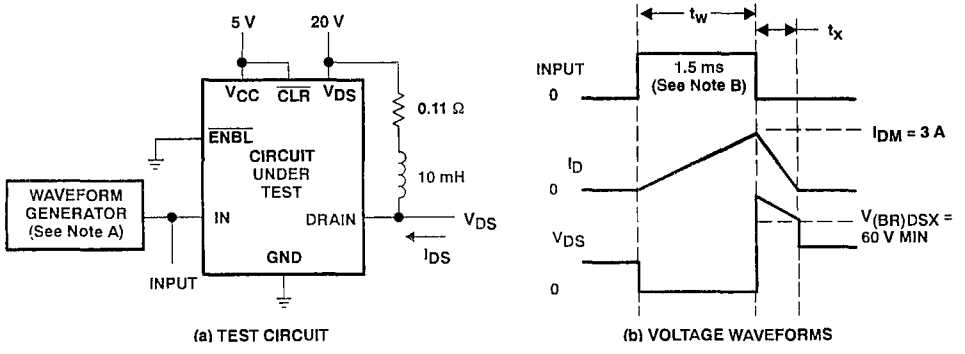


FIGURE 3. REVERSE-RECOVERY-CURRENT WAVEFORMS OF SOURCE-DRAIN DIODE

PARAMETER MEASUREMENT INFORMATION



(a) TEST CIRCUIT (b) VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 1$ ms, PRR = 5 kHz, $Z_O = 50\ \Omega$.
B. Input pulse duration is increased until peak current $I_{DM} = 3$ A.

Energy test level is defined as $E_{AS} = \dfrac{I_{DM} \times V_{(BR)DSX} \times t_x}{2} = 50$ mJ min.

FIGURE 4. SINGLE-PULSE AVALANCHE ENERGY TEST CIRCUIT AND WAVEFORMS

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MAXIMUM RATINGS

MAXIMUM DRAIN CURRENT
vs
DUTY CYCLE

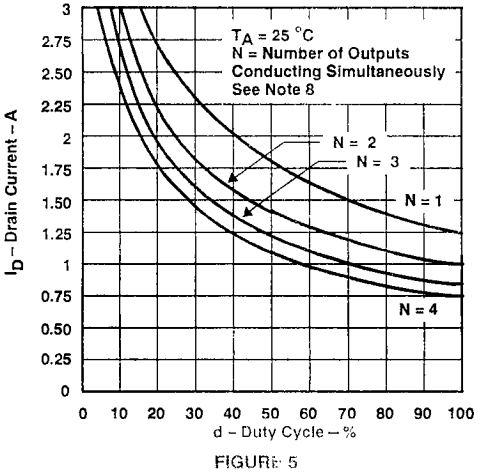


FIGURE 5

MAXIMUM DRAIN CURRENT
vs
DUTY CYCLE

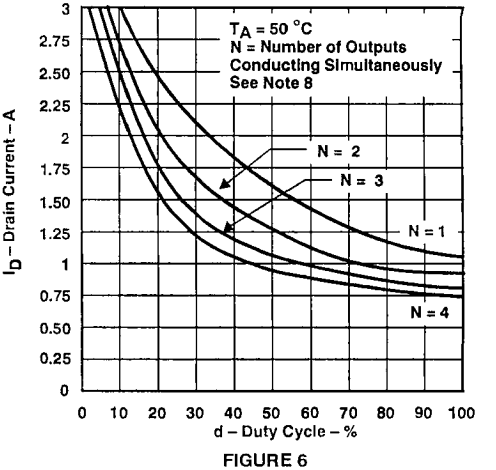


FIGURE 6

MAXIMUM DRAIN CURRENT
vs
DUTY CYCLE

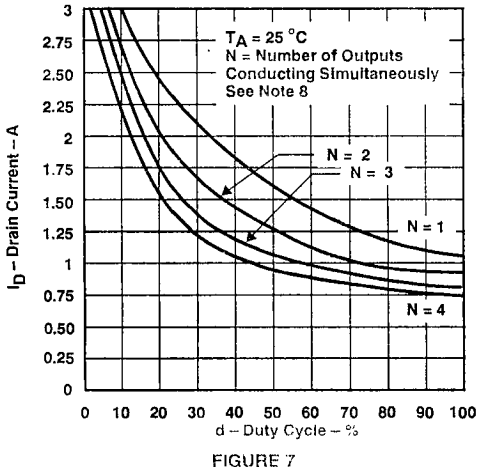


FIGURE 7

MAXIMUM DRAIN CURRENT
vs
PULSE DURATION

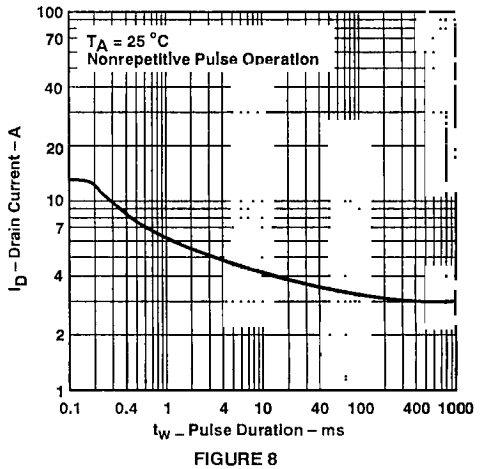
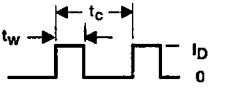


FIGURE 8

NOTE 8: For Figures 5, 6, and 7, $d = \frac{t_W}{t_C} = \frac{10\ ms}{t_C}$. Where t_W and t_C are defined by the following:



MAXIMUM RATINGS

MAXIMUM CONTINUOUS
DRAIN CURRENT
vs
FREE-AIR TEMPERATURE

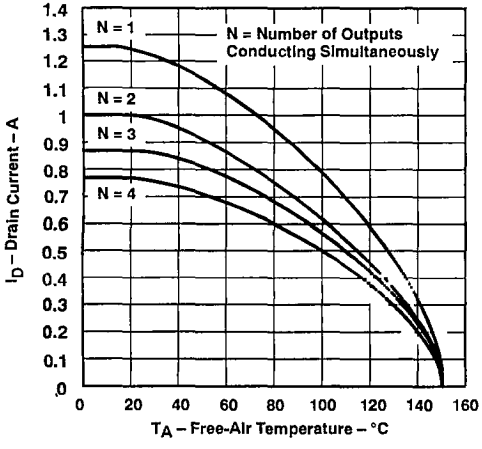


FIGURE 9

FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

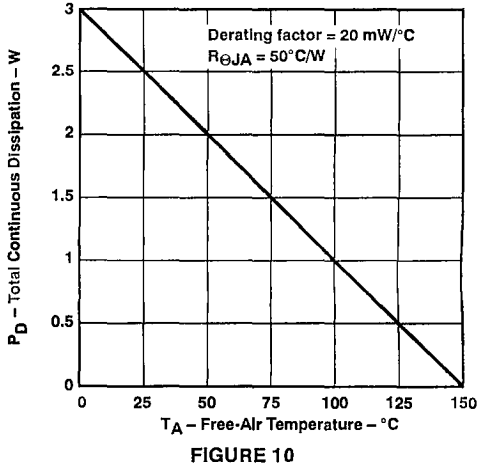


FIGURE 10

TRANSIENT THERMAL IMPEDANCE
vs
ON TIME

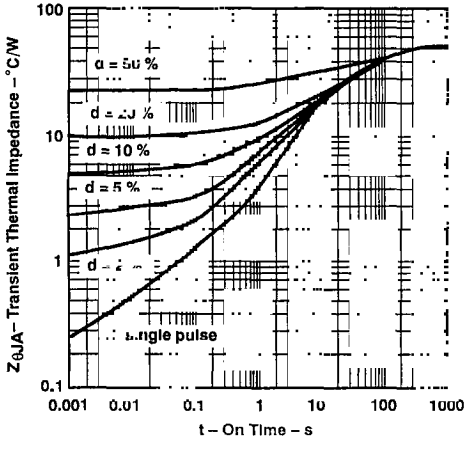


FIGURE 11

The single-pulse curve in Figure 11 represents measured data. The curves for various pulse durations are based on the following equation:

$$Z_{\theta JA} = \left| \frac{t_w}{t_c} \right| R_{\theta JA} + \left| 1 - \frac{t_w}{t_c} \right| Z_{\theta(t_w + t_c)} + Z_{\theta(t_w)} - Z_{\theta(t_c)}$$

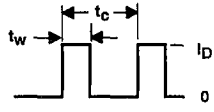
Where:

$Z_{\theta(t_w)}$ = the single-pulse thermal impedance for t = t_w seconds

$Z_{\theta(t_c)}$ = the single-pulse thermal impedance for t = t_c seconds

$Z_{\theta(t_w + t_c)}$ = the single-pulse thermal impedance for t = $t_w + t_c$ seconds

d = t_w/t_c



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TYPICAL CHARACTERISTICS

STATIC DRAIN-SOURCE
ON-RESISTANCE
vs
DRAIN CURRENT

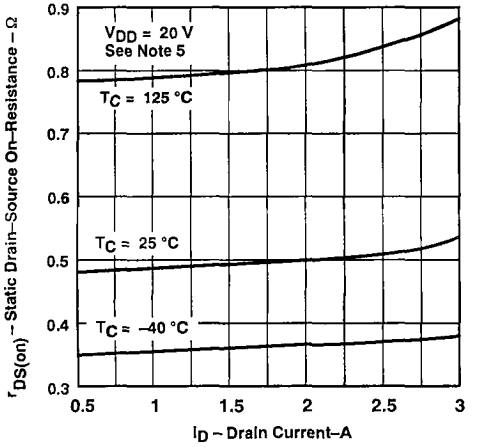


FIGURE 12

STATIC DRAIN-SOURCE
ON-RESISTANCE
vs
POWER MOSFET DRIVER SUPPLY VOLTAGE

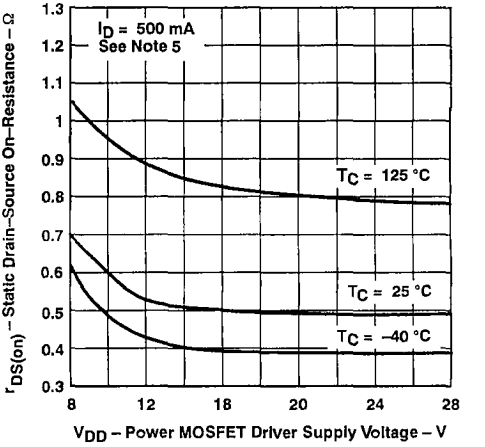


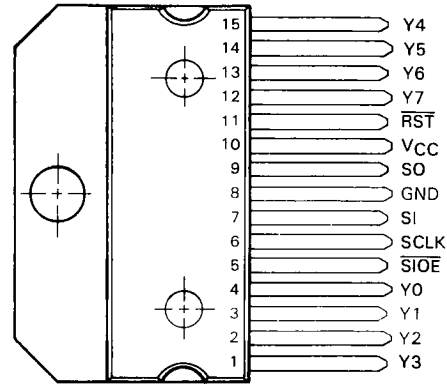
FIGURE 13

NOTE 5: Technique should limit $T_j - T_C$ to 10°C maximum.

D3282, AUGUST 1989 - ED JUNE 1990

- 8-Bit Serial-In Parallel-Out Driver
- 1-A Output Current Capability per Channel or 8-A Total Current
- Over-Current Limiting and Out-of-Saturation Voltage Protection on Driver Outputs
- Contains Eight Open-Collector Saturating Sink Outputs with Low On-State Voltage
- High-Impedance Inputs with Hysteresis are Compatible with TTL or CMOS Levels
- Very Low Standby Power . . . 20 mW Typical
- Status of Output Drivers May Be Monitored at Serial Output
- 3-State Serial Output Permits Serial Cascading or Wire-AND Device Connections
- 25-V Transient Clamping with Inductive Switching on Outputs, 40-mJ Rating per Driver Output

KV PLASTIC PACKAGE
(TOP VIEW)



The tab is electrically connected to pin 8.

description

The TPIC2801 is a monolithic BIDFET† integrated circuit that is designed to sink currents up to 1 A at 30 V simultaneously at each of eight driver outputs under serial input data control. Status of the individual driver outputs is available in serial data format. The driver outputs have overcurrent limiting and out-of-saturation voltage protection features. Applications include driving solenoids, relays, dc motors, lamps, and other medium-current or high-voltage loads.

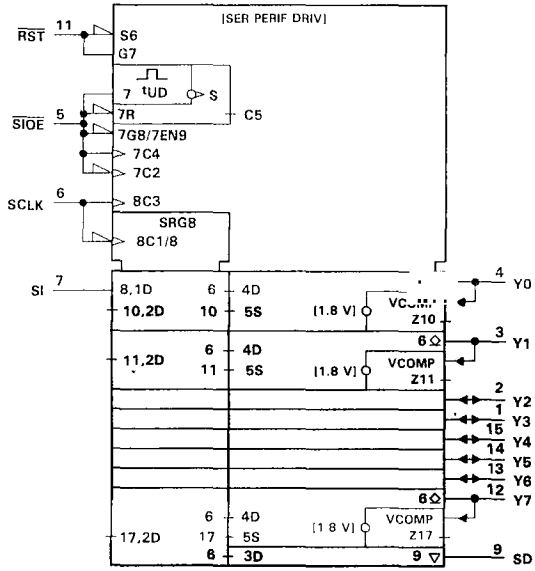
The device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit parallel latch, which independently controls each of the eight Y-output drivers.

Data is entered into the device serially via the serial input (SI) and goes directly into the lowest bit (0) of the shift register. Using proper timing signals, the input data is passed to the corresponding output latch and output driver. A logic high bit at SI_n turns the corresponding output driver (Y_n) off. A logic low bit at SI turns the corresponding output driver on. Serial data is transferred into SI on the high-to-low transition of serial clock (SCLK) input in 8-bit bytes with data for Y7 output first (MSB) and data for Y0 output (LSB) last. Both SI and SCLK are active when serial input-output enable ($\overline{SIOE}$) input is low and are disabled when $\overline{SIOE}$ is high.

Each driver output is monitored by a voltage comparator that compares the Y-output voltage level with an internal out-of-saturation threshold voltage reference level. The logic state of the comparator output is dependent upon whether the Y output is greater or smaller than the reference voltage level. An activated driver output will be unlatched and turned off when the output voltage exceeds the out-of-saturation threshold voltage level except when the internal unlatch enable is low and disabled. The high-to-low transition of $\overline{SIOE}$ transfers the logic state of the comparator output to the shift register.

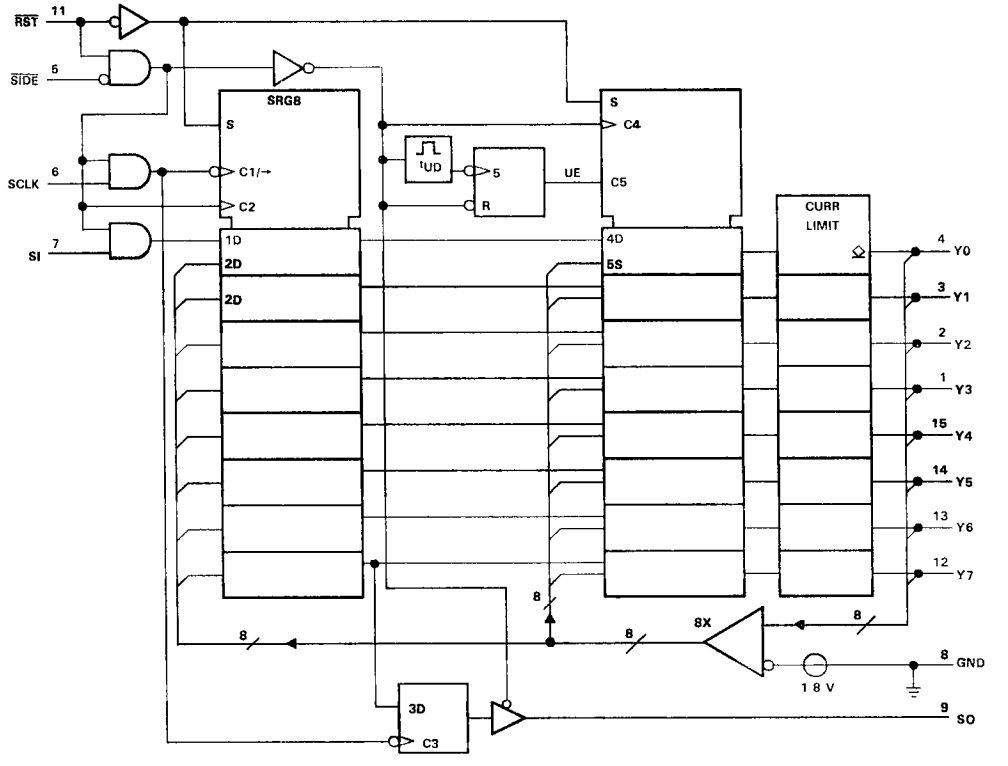
† BIDFET – Bipolardouble-diffused, N-channel and P-channel MOS transistors on same chip – patented process.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



PIN NAME	PIN NO.	I/O	DESCRIPTION
GND	8		Ground. Common return for entire chip. The current out of this pin is potentially as high as 4 A if all outputs are on. This ground is used for both logic and power circuits
$\overline{RST}$	11	I	Reset. An asynchronous reset is provided for the shift register and the parallel latches. This pin is active when low and has no internal pullup. When active, it causes the power outputs to turn off. A power-on clear can be implemented using an RC network to V_{CC}.
$\overline{SCLK}$	6	I	Serial Clock. This pin clocks the shift register. The serial output (SO) will change state on the rising edge of this clock and serial input (SI) data will be accepted on the falling edge.
SI	7	I	Serial Input. This pin is the serial data input. A high on this pin will program a particular output to be off and a low will turn it on.
$\overline{SIOE}$	5	I	Serial Input-Output Enable. Data is transferred from the shift registers to the power outputs on the rising edge of this signal. The falling edge of this signal parallel loads the output voltage sense bits from the power outputs into the shift register. The output driver for the serial output (SO) pin is enabled when this pin is low, provided is high.
SO	9	O	Serial Output. This pin is the serial 3-state output from the shift register and is in a high-impedance state when $\overline{SIOE}$ is high or $\overline{RST}$ is low. A high for a data bit on this pin indicates that the corresponding power output (Y_n) is high. This could mean that the output was programmed to be off the last time a byte was input to the device or that the output faulted and was latched off by the output voltage sense indicator. A low on this pin for a data bit indicates that the corresponding power output (Y_n) is low (an "on" output stage or open-circuit condition).
V_{CC}	10		5-V supply voltage
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7	4 3 2 1 15 14 13 12	O	Power Outputs. The outputs are provided with current limiting and voltage sense for fault indication and protection. The nominal load current for these outputs is 500 mA, but the current limiting is set to a minimum of 1.2 A. The active-low outputs also have voltage clamps set at about 35 V for recirculation of inductive load current. Internal 90-kΩ pull-down resistors are provided at each output. These resistors hold the output low during an open-circuit condition.

PRINCIPLES OF OPERATION

timing data transfer

Figure 1 shows the overall 8-bit data-byte transfer to and from the TPIC2801 interface bus. The logic state of the eight output drivers, Y0 through Y7, is latched into the shift register at time t_0 on the high-to-low transition of $\overline{SIOE}$. Therefore, the SO output data (DY0, DY1 . . .) represents the conditions at the Y-driver outputs at time t_0. The data at SO output is updated on the low-to-high transition of SCLK.

Input data present at the SI input is clocked into the shift register on the high-to-low transition of SCLK. As shown in Figure 1 on the SI input, input data DI7 is clocked in at time t_1, DI6 is clocked in at time t_2, etc. Eight SCLK pulses are used to serially load the eight bits of new data into the device. After all the new data is serially loaded, the low-to-high transition of $\overline{SIOE}$ parallel loads the new data to the eight driver output latches, which in turn directly control the eight Y-driver outputs.

An unlimited amount of data can be shifted through the shift register (into the SI and out the SO) and this allows other devices to be cascaded in a daisy chain with the TPIC2801. Once the last data bit has been shifted into the TPIC2801, the $\overline{SIOE}$ input should be pulled high. The clock (SCLK) input should be low at both transitions of the $\overline{SIOE}$ input to avoid any false clocking of the shift register. The SCLK input is gated by the $\overline{SIOE}$ input, so the SCLK input is ignored whenever the $\overline{SIOE}$ is high. At the rising edge of the $\overline{SIOE}$ input, the shift register data is latched into the parallel latch and the output stages will be actuated by the new data. An internal 100-μs delay timer is also started on this rising edge. During the time delay, the outputs will be protected only by the analog current-limiting circuits, since the resetting of the parallel latches by fault conditions will be inhibited during this time period. This allows the device to overcome any high switching currents that can flow during turn-on. Once the delay has ended, the output voltages are sensed by the comparators and any output voltages higher than nominally 1.8 V are latched off.

PRINCIPLES OF OPERATION

fault-conditions check

Open-circuit conditions on any output can be monitored or checked by programming that output off. After a short delay (microseconds), another control byte can be clocked into the the device. If the diagnostic bit for that output comes back as a low, it indicates that the output is low and open circuited. A current overload condition can be detected by programming an output on. After waiting an appropriate length of time, another byte should be clocked into the TPIC2801. The diagnostic bit clocked back from the TPIC2801 in the subsequent data transfer should indicate a low output. If a high returns, a current overload is indicated. A quick overall check can be done by clocking in a test control byte. After a sufficient time delay, another control byte (same byte can be used) is clocked in. The diagnostic data is exclusive ORed with the original control byte. If a fault condition exists, a high will result.

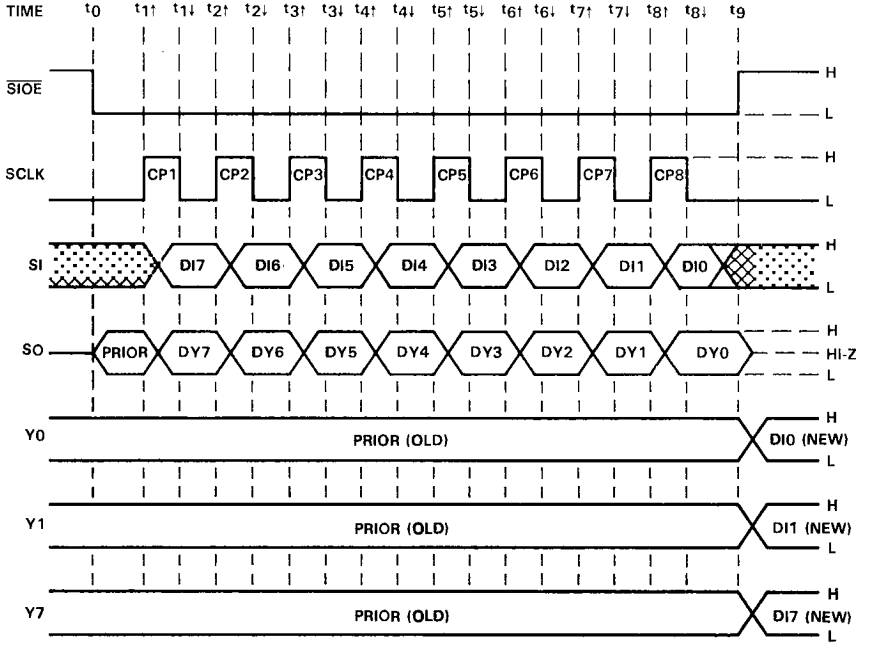
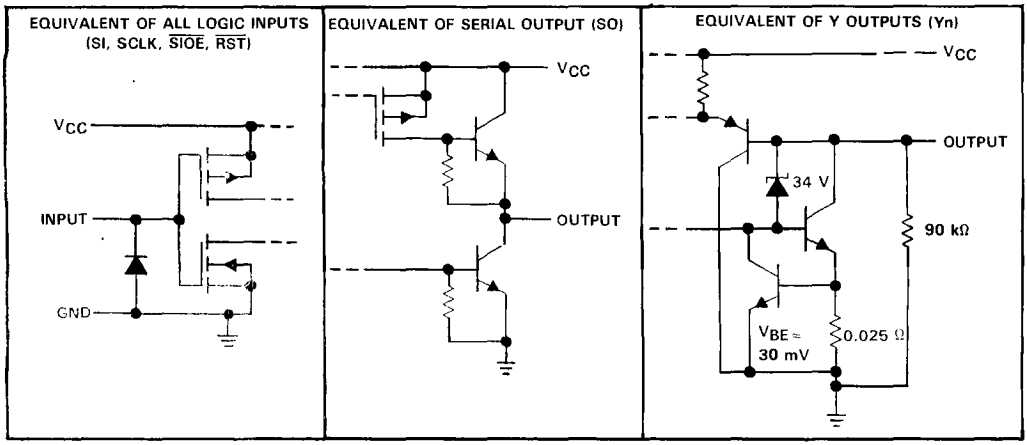


FIGURE 1. DATA-BYTE TRANSFER TIMING

schematics of inputs and outputs



All resistor and voltage values shown are nominal.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1)	−0.3 V to 7 V
Input voltage, V_I	7 V
Output voltage range at SO	−0.3 V to 7 V
Input current, I_I	−15 mA
Peak output sink current at Y, I_O repetitive, t_W = 10 ms, duty cycle = 50%, see Notes 2 and 3	Internally Limited
Continuous output current at Y, I_O (see Note 3)	1 A
Peak current through GND terminal:	
Nonrepetitive t_W = 0.2 ms	−8 A
Repetitive, t_W = 10 ms, duty cycle = 50%	−6 A
Continuous current through GND terminal	−4.5 A
Output clamp energy, E_{OK} (after turning off $I_{O(on)}$ = 0.5 A)	40 mJ
Continuous dissipation at (or below) 25°C free-air temperature (see Note 4)	3.575 W
Continuous dissipation at (or below) 75°C case temperature (see Note 4)	25 W
Operating case or virtual-junction temperature range	−55°C to 150°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. Each Y output is individually current limited with a typical over-current limit of about 1.4 A.
3. Multiple Y outputs of this device may conduct rated current simultaneously; however, power dissipation (average) over a short time interval must fall within the continuous dissipation range and the GND current must fall within the GND-terminal current range.
4. For operation above 25°C free-air temperature, derate linearly at the rate of 28.6 mW/°C. For operation above 75°C case temperature, derate lineraly at the rate of 333 mW/°C. To avoid exceeding the maximum virtual-junction temperature, these ratings must not be exceeded.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	0.7 V_{CC}		5.25	V
Low-level input voltage, V_{IL}	−0.3		0.2 V_{CC}	V
Output voltage, $V_{O(off)}$			30	V
Continuous output current, $I_{O(on)}$			1	A
Operating case temperature, T_C	−40	25	105	°C

timing requirements (see Figure 2)

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	MAX	UNIT
f_{SCLK}	Clock frequency				0	500	kHz
t_{wSCLKH}	Pulse duration, SCLK high				840		ns
t_{wSCLKL}	Pulse duration, SCLK low				840		ns
t_{wRST}	Pulse duration, $\overline{RST}$ low				1000		ns
t_{su1}	Setup time	$\overline{SIOE}$↓	SCLK↑		1000		ns
t_{su2}	Setup time	SCLK↓	$\overline{SIOE}$↑		1000		ns
t_{su3}	Setup time	SI	SCLK↓		500		ns
t_{h1}	Hold time	SCLK↓	SI		500		ns
t_r	Rise time (SCLK, SI, $\overline{SIOE}$)					2	µs
t_f	Fall time (SCLK, SI, $\overline{SIOE}$)					2	µs

electrical characateristics over recommended ranges of supply voltage and operating case temperature (unless otherwise noted)

driver array outputs (Y0 to Y7)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OK}	Output clamp voltage	I_O = 0.5 A, output programmed on and current shunted to ground		30	36	40	V
$I_{O(off)}$	Off-state output current	V_O = 24 V with output programmed off				1	mA
$I_{O(CL)}$	Output current limit	V_O = 3 V with output programmed on		1.05	1.4		A
$V_{O(on)}$	On-state output voltage	With output programmed on	I_{OL} = 0.5 A		0.4	0.5	V
			I_{OL} = 0.75 A		0.6	1	V
			I_{OL} = 1 A, During unlatch disable		0.8	1.5	V
V_{TOS}	Out of saturation threshold voltage	With output programmed on and an over-current fault condition		1.6	1.8	2	V

shift register (inputs SI, $\overline{SIOE}$, SCLK, and $\overline{RST}$)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{T+}	Positive-going threshold voltage			0.7 V_{CC}	V
V_{T-}	Negative-going threshold voltage		0.2 V_{CC}		V
V_{hys}	Hysteresis voltage ($V_{T+} - V_{T-}$)		0.85	2.25	V
I_i	Input current	V_I = 0 to V_{CC}		±10	µA
C_i	Input capacitance	V_I = 0 to V_{CC}		20	pF

† All typical values are at V_{CC} = 5 V, T_J = 25°C.

electrical characteristics over recommended ranges of supply voltage and operating case temperature (unless otherwise noted)

shift register (output SO)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OL}	Low-level output voltage	I_O = 1.6 mA			0.2	0.4	V
V_{OH}	High-level output voltage	I_O = −0.8 mA		V_{CC} −1.3			V
I_D	Output current	V_D = 0 to V_{CC}, $\overline{SIOE}$ input high				±10	µA
I_{CC}	Supply current	All outputs on, I_O = 0.5 A at all outputs	T_J = 105°C			150	mA
			T_J = 25°C			200	
			T_J = −40°C			250	
I_{CC}	Supply current	All outputs off	T_J = 25°C		4	10	mA
C_O	Output capacitance	V_O = 0 to V_{CC}, $\overline{SIOE}$ input high				20	pF

† All typical values are at V_{CC} = 5 V, T_J = 25°C.

thermal characteristics

PARAMETER		MIN	MAX	UNIT
$R_{\theta JC}$	Thermal resistance, junction-to-case temperature		3	°C/W
$R_{\theta JA}$	Thermal resistance, junction-to-ambient temperature		35	°C/W

switching characteristics over recommended ranges of supply voltage and operating case temperatures (unless otherwise noted)

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	MAX	UNIT
t_{en}	Enable time	$\overline{SIOE}$↓	SD	C_L = 20 pF, See Figure 3 R_L = 2 kΩ,		1000	ns
t_{dis}	Disable time	$\overline{SIOE}$↑	SO	C_L = 20 pF, See Figure 3 R_L = 2 kΩ,		1000	ns
t_{d1}	Delay time, valid data	SCLK↑	SO	C_L = 200 pF, See Figure 4		740	ns
t_{d2}	Delay time, unlatch disable	$\overline{SIOE}$↑	Y_n	C_L = 20 pF, See Figure 5 R_L = 5 Ω,	75	250	µs
$t_{r(so)}$	Rise time, SO			C_L = 200 pF, See Figure 4		150	ns
$t_{f(so)}$	Fall time, SO			C_L = 200 pF, See Figure 4		150	ns
$t_{d(on)}$	Delay time, turn-on	$\overline{SIOE}$↑	Y_n	I_{OL} = 500 mA, R_L = 28 Ω, C_L = 20 pF, See Figure 6		10	µs
$t_{d(off)}$	Delay time, turn-off	$\overline{SIOE}$↑	Y_n	I_{OL} = 500 mA, R_L = 28 Ω, C_L = 20 pF, See Figure 6		10	µs
t_v	Valid time, SO output data remains valid after SCLK high	SCLK↑	SO	C_L = 200 pF, See Figure 4	0		ns

PARAMETER MEASUREMENT INFORMATION

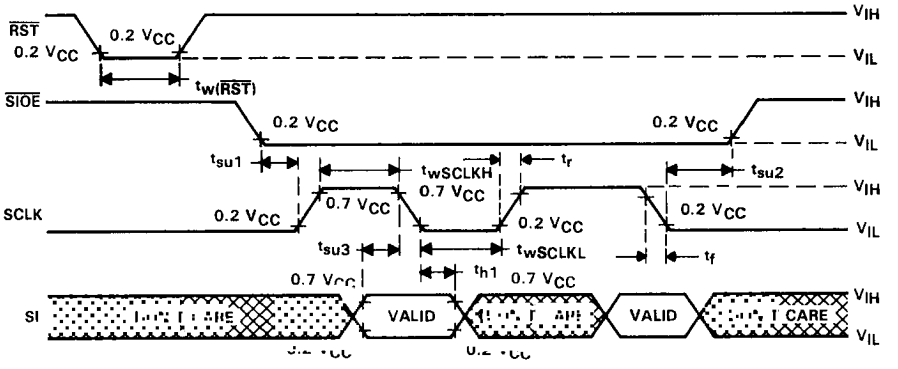
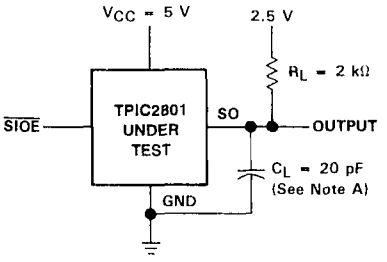
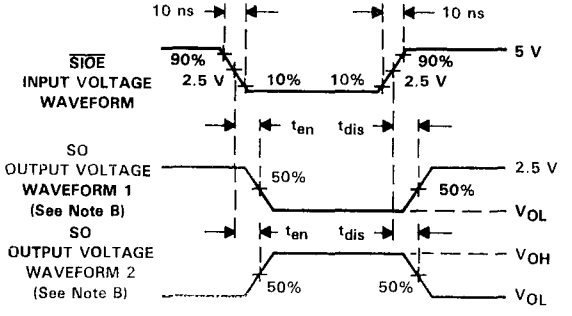


FIGURE 2. INPUT TIMING WAVEFORMS

PARAMETER MEASUREMENT INFORMATION



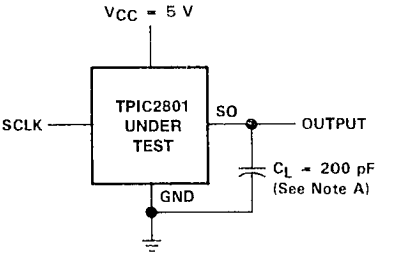
TEST CIRCUIT FOR ENABLE AND DISABLE TIMES



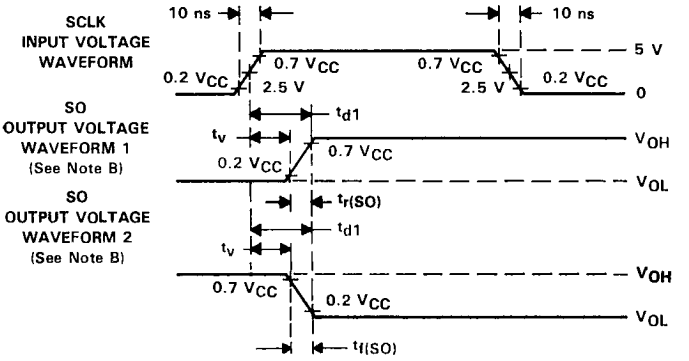
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control when $\overline{SIOE}$ is high. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control when $\overline{SIOE}$ is high.

FIGURE 3. VOLTAGE WAVEFORMS FOR ENABLE AND DISABLE TIMES

PARAMETER MEASUREMENT INFORMATION



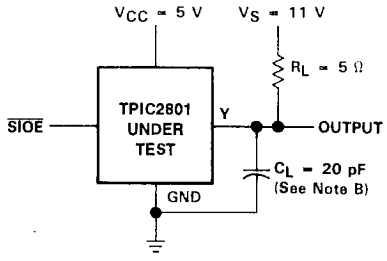
TEST CIRCUIT FOR VALID DATA
DELAY TIME t_{d1} AND VALID TIME t_v



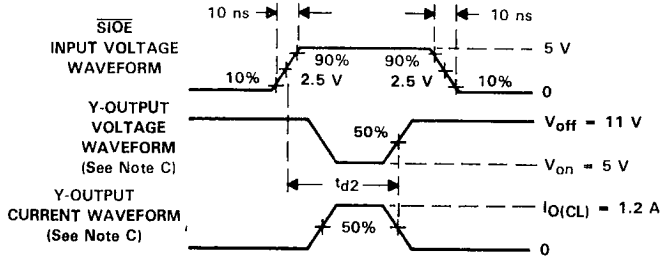
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the low-to-high transition of SCLK causes the SO output to switch from low to high. Waveform 2 is for an output with internal conditions such that the low-to-high transition of SCLK causes the SO output to switch from high to low.

FIGURE 4. VOLTAGE WAVEFORMS FOR DELAY TIMES

PARAMETER MEASUREMENT INFORMATION



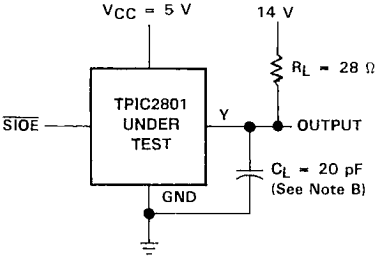
TEST CIRCUIT FOR UNLATCH DISABLE
DELAY TIME t_{d2}
(See Note A)



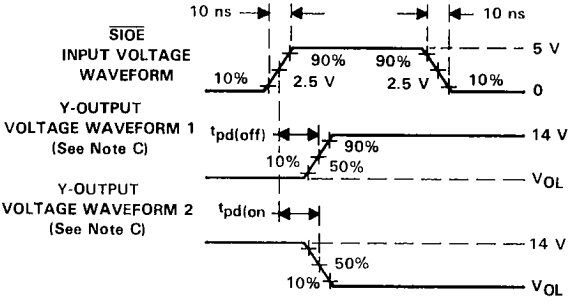
NOTES: A. t_{d2} = delay until Y-output current goes off under fault condition.
B. C_L includes probe and jig capacitance.
C. Output voltage and current waveforms are for an output with internal conditions such that the low-to-high transition of $\overline{SIOE}$ causes the output to switch from being off to being on.
D. Load voltage V_S and load resistance R_L are selected such that on-state voltage at the Y output under test, V_{on} is greater than the maximum out-of-saturation threshold voltage, V_{TOS}. Thus, $V_{OL} = V_{on} > V_{TOS(max)} = 1.98$ V.

FIGURE 5. VOLTAGE AND CURRENT WAVEFORMS FOR UNLATCH DISABLE DELAY

PARAMETER MEASUREMENT INFORMATION



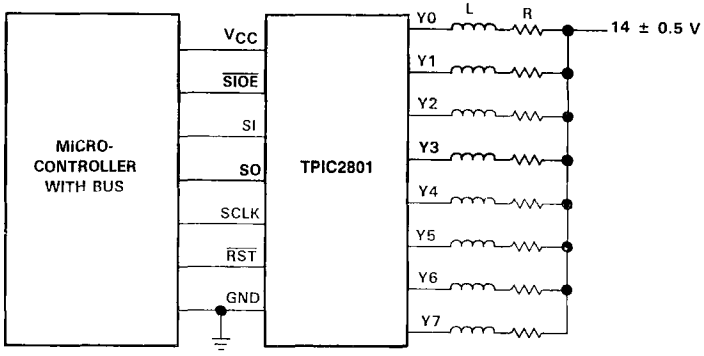
TEST CIRCUIT FOR TURN-OFF AND TURN-ON $t_{d(on)}$ DELAY TIMES
(See Note A)



NOTES: A. $t_{d(off)} = t_{PLH}$, $t_{d(on)} = t_{PHL}$.
B. C_L includes probe and jig capacitance.
C. Waveform 1 is for an output with internal conditions such that the low-to-high transition of SIOE causes the output to switch from on to off. Waveform 2 is for an output with internal conditions such the low-to-high transition of SIOE causes the output to switch from off to on.

FIGURE 6. VOLTAGE WAVEFORMS FOR TURN-OFF AND TURN-ON DELAY TIMES

TYPICAL APPLICATION DATA



V_{CC} = 5 V ± 5%
R = 30 Ω ± 5%
L = 10 mH ± 10%
8 LOADS UP TO 0.5 A EACH

FIGURE 7. MICROCONTROLLER DRIVING EIGHT LOADS USING A TPIC2801 FOR LOAD INTERFACE

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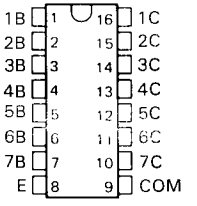
D2624, DECEMBER 1976—REVISED SEPTEMBER 1986

HIGH-VOLTAGE HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

- 500-mA Rated Collector Current (Single Output)
- High-Voltage Outputs . . . 50 V
- Output Clamp Diodes
- Inputs Compatible With Various Types of Logic
- Relay Driver Applications
- Designed to Be Interchangeable With Sprague ULN2001A Series

D OR N PACKAGE
(TOP VIEW)

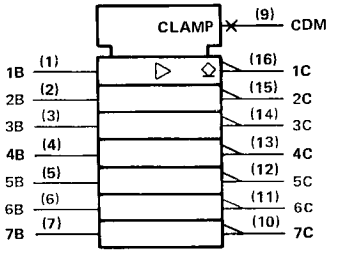


description

The ULN2001A, ULN2002A, ULN2003A, ULN2004A, and ULN2005A are monolithic high-voltage, high-current Darlington transistor arrays. Each consists of seven n-p-n Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of a single Darlington pair is 500 mA. The Darlington pairs may be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. For 100-V (otherwise interchangeable) versions, see the SN75465 through SN75469.

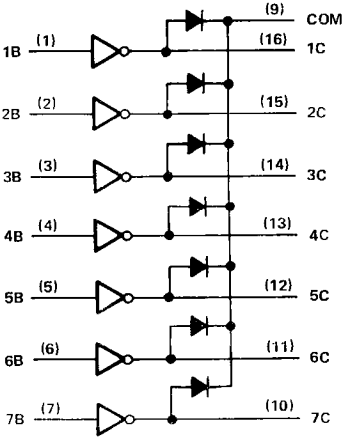
The ULN2001A is a general-purpose array and may be used with TTL, P-MOS, CMOS, and other MOS technologies. The ULN2002A is specifically designed for use with 14- to 25-V P-MOS devices. Each input of this device has a zener diode and resistor in series to control the input current to a safe limit. The ULN2003A has a 2.7-kΩ series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices. The ULN2004A has a 10.5-kΩ series base resistor to allow its operation directly from CMOS or P-MOS devices that use supply voltages of 6 to 15 V. The required input current of the ULN2004A is below that of the ULN2003A, and the required voltage is less than that required by the ULN2002A. The ULN2005A has a 1050-Ω series base resistor and is specifically designed for use with TTL devices where higher output current is required and loading of the driving source is not a concern.

logic symbol†

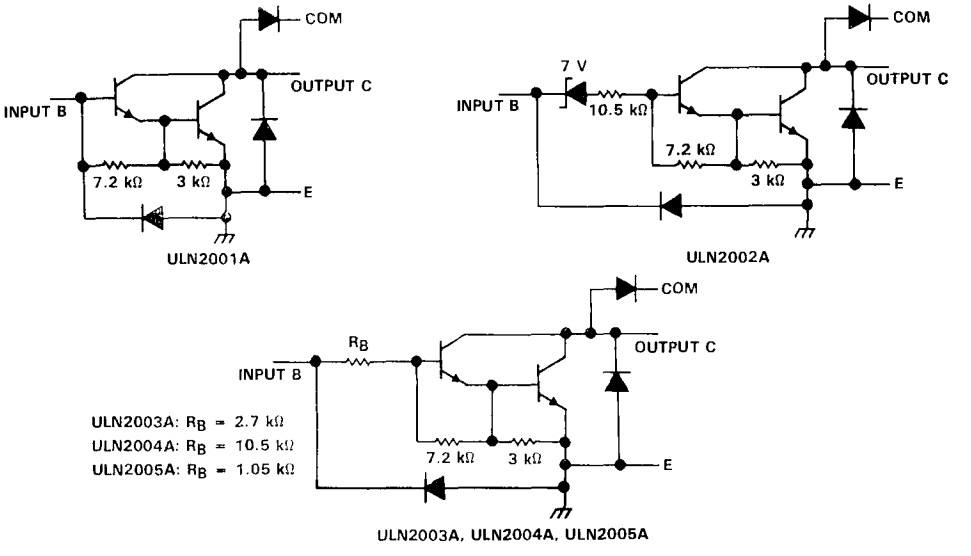


†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram



schematics (each Darlington pair)



All resistor values shown are nominal.

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Collector-emitter voltage	50 V
Input voltage (see Note 1): ULN2002A, ULN2003A, ULN2004A	30 V
ULN2005A	15 V
Peak collector current (see Figures 14 and 15)	500 mA
Output clamp diode current	500 mA
Total emitter-terminal current	−2.5 A
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range	−20°C to 85°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

NOTE 1: All voltage values are with respect to the emitter/substrate terminal, E, unless otherwise noted.

DISSIPATION RATING TABLE

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
D	950 mW	7.6 mW/°C	494 mW
N	1150 mW	9.2 mW/°C	598 mW

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	ULN2001A			ULN2002A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
I_{CEX}	Collector cutoff current	1	V_{CE} = 50 V, I_I = 0			50			50	μA
			V_{CE} = 50 V, I_I = 0			100			100	
		2	T_A = 70°C, V_I = 6 V						500	
$I_{I(off)}$	Off-state input current	3	V_{CE} = 50 V, I_C = 500 μA, T_A = 70°C	50	65		50	65		μA
I_I	Input current	4	V_I = 17 V					0.82	1.25	mA
h_{FE}	Static forward current transfer ratio	5	V_{CE} = 2 V, I_C = 350 mA	1000						
$V_{I(on)}$	On-state input voltage	6	V_{CE} = 2 V, I_C = · mA						13	V
$V_{CE(sat)}$	Collector-emitter saturation voltage	5	I_I = 250 μA, I_C = : mA		0.9	1.1		0.9	1.1	V
			I_I = μA, I_C = · mA		1	1.3		1	1.3	
			I_I = μA, I_C = · mA		1.2	1.6		1.2	1.6	
I_R	Clamp diode reverse current	7	V_R = 50 V			50			50	μA
			V_R = 50 V, T_A = 70°C			100				
V_F	Clamp diode forward voltage	8	I_F = 350 mA		1.7	2		1.7		V
C_i	Input capacitance		V_I = 0, f = 1 MHz		15	25		15	25	pF

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	ULN2003A			ULN2004A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
I_{CEX}	Collector cutoff current	1	V_{CE} = 50 V, I_I = 0			50			[illegible]	μA
			V_{CE} = 50 V, I_I = 0			100			100	
		2	T_A = 70°C, V_I = 1 V						[illegible]	
$I_{I(off)}$	Off-state input current	3	V_{CE} = 50 V, I_C = 500 μA, T_A = 70°C	50	65		50	65		μA
I_I	Input current	4	V_I = 3.85 V		0.93	1.35				mA
			V_I = 5 V					0.35	0.5	
			V_I = 12 V					1	1.45	
$V_{I(on)}$	On-state input voltage	6	V_{CE} = 2 V, I_C = 125 mA						5	V
			I_C = 200 mA			2.4			6	
			I_C = · mA			2.7				
			I_C = · mA						7	
			I_C = 300 mA			3				
			I_C = mA						8	
$V_{CE(sat)}$	Collector-emitter saturation voltage	5	I_I = 250 μA, I_C = 100 mA		0.9	1.1		0.9	1.1	V
			I_I = 350 μA, I_C = 200 mA		1	1.3		1	1.3	
			I_I = 500 μA, I_C = mA		1.2	1.6		1.2	1.6	
I_R	Clamp diode reverse current	7	V_R = 50 V			50			50	μA
			V_R = 50 V, T_A = 70°C			100				
V_F	Clamp diode forward voltage	8	I_F = mA		1.7	2		1.7		V
C_i	Input capacitance		V_I = 0, f = 1 MHz		15	25		15	25	pF

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	ULN2001A MIN	ULN2001A TYP	ULN2001A MAX	UNIT
I_{CEX}	Collector cutoff current	1	V_{CE} = 50 V, I_I = 0			50	μA
			V_{CE} = 50 V, I_I = 0, T_A = 70°C			[illegible]	
$I_{I(off)}$	Off-state input current	3	V_{CE} = 50 V, I_C = 500 μA, T_A = 70°C	50	65		μA
I_I	Input current	4	V_I = 3 V		1.5	2.4	mA
$V_{I(on)}$	On-state input voltage	6	V_{CE} = 2 V, I_C = 350 mA			2.4	V
$V_{CE(sat)}$	Collector-emitter saturation voltage	5	I_I = 250 μA, I_C = [illegible] mA		0.9	1.1	V
			I_I = [illegible] μA, I_C = [illegible] mA		1	1.3	
			I_I = [illegible] μA, I_C = [illegible] mA		1.2	1.6	
I_R	Clamp diode reverse current	7	V_R = 50 V			50	μA
			V_R = 50 V, T_A = 70°C			100	
V_F	Clamp diode forward voltage	8	I_F = 350 mA		1.7	2	V
C_i	Input capacitance		V_I = 0, f = 1 MHz		15	25	pF

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 9		0.25	1	μs
t_{PHL}	Propagation delay time, high-to-low-level output			0.25	1	μs
V_{OH}	High-level output voltage after switching	V_S = 50 V, I_O = 300 mA, See Figure 10	V_S − 20			mV

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PARAMETER MEASUREMENT INFORMATION

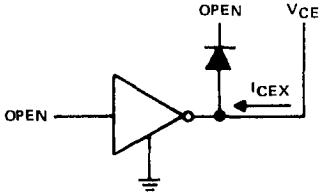


FIGURE 1. I_{CEX}

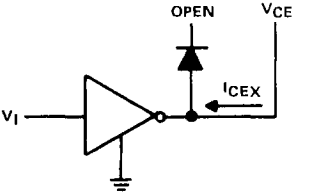


FIGURE 2. I_{CEX}

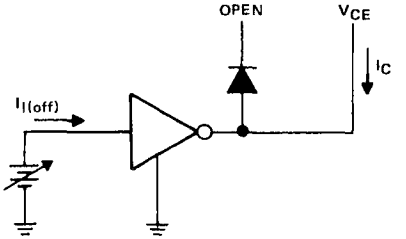


FIGURE 3. $I_{I(off)}$

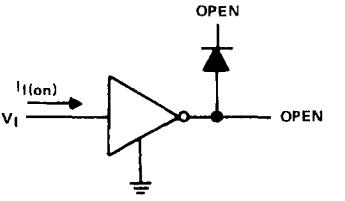
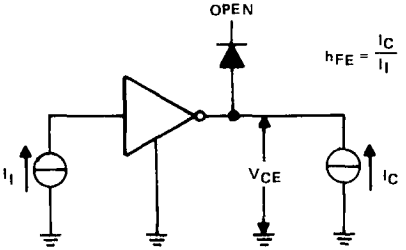


FIGURE 4. I_I



NOTE: I_I is fixed for measuring $V_{CE(sat)}$, variable for measuring h_{FE}.

FIGURE 5. h_{FE}, $V_{CE(sat)}$

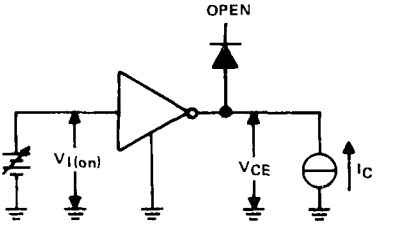


FIGURE 6. $V_{I(on)}$

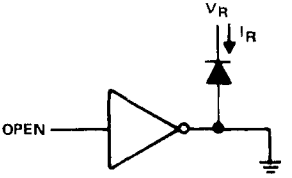


FIGURE 7. I_R

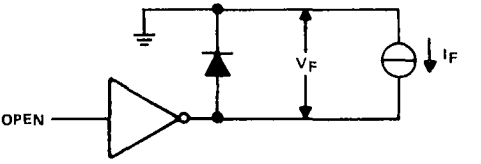
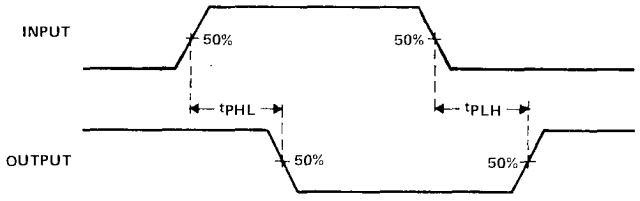


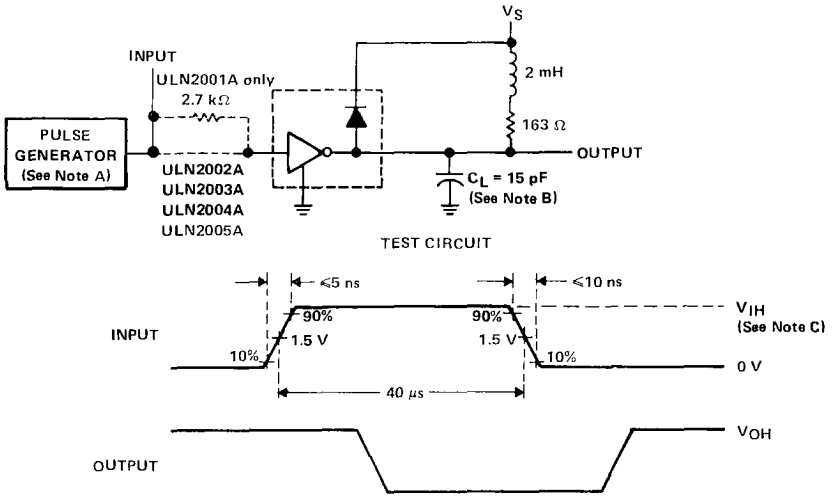
FIGURE 8. V_F

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

FIGURE 9. PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_o = 50 Ω.
B. C_L includes probe and jig capacitance.
C. For testing the ULN2001A, ULN2003A, and the ULN2005A, V_{IH} = 3 V; for the ULN2002A, V_{IH} = 13 V; for the ULN2004A, V_{IH} = 8 V.

FIGURE 10. LATCH-UP TEST

TYPICAL CHARACTERISTICS

COLLECTOR-EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT (ONE DARLINGTON)

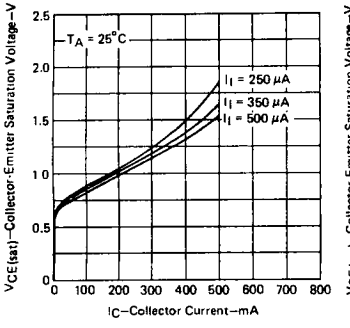


FIGURE 11

COLLECTOR EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT (TWO DARLINGTONS PARALLELED)

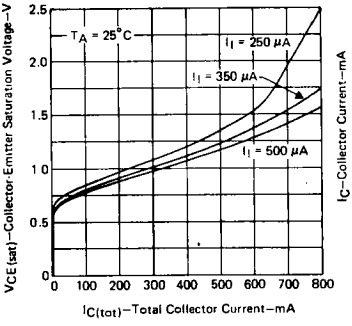


FIGURE 12

COLLECTOR CURRENT vs INPUT CURRENT

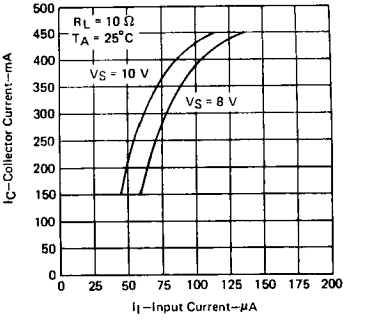


FIGURE 13

THERMAL INFORMATION

D PACKAGE MAXIMUM COLLECTOR CURRENT vs DUTY CYCLE

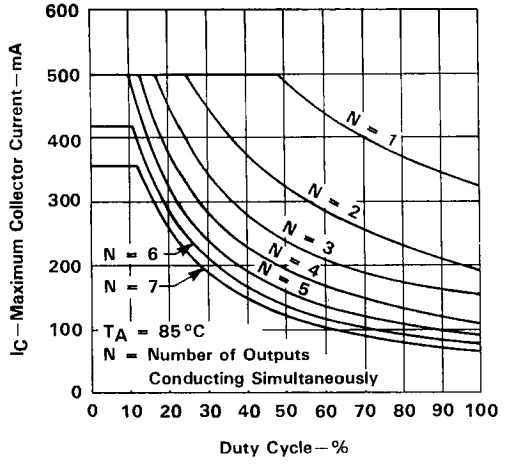


FIGURE 14

N PACKAGE MAXIMUM COLLECTOR CURRENT vs DUTY CYCLE

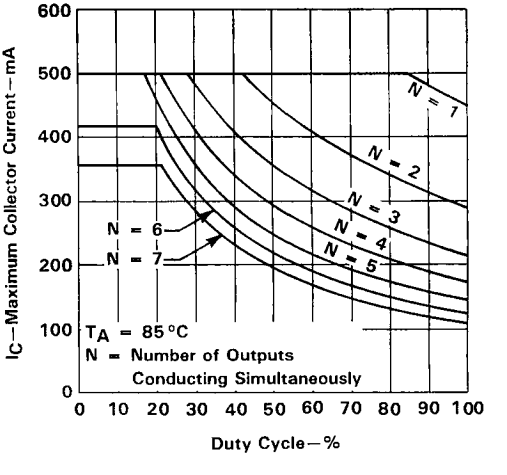
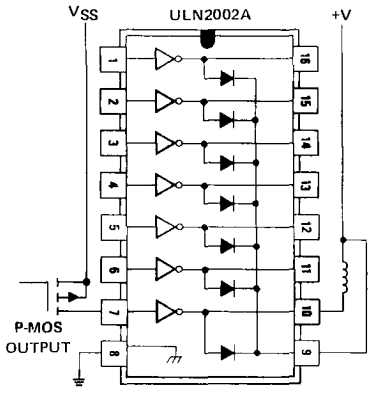
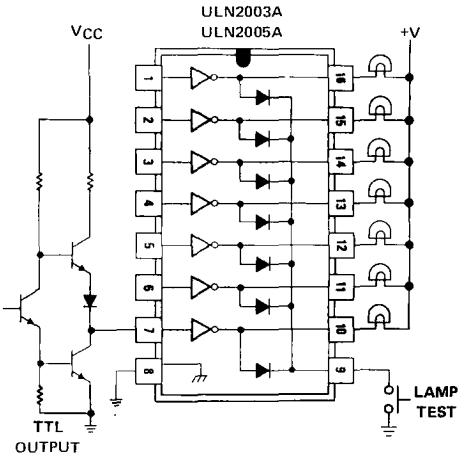


FIGURE 15

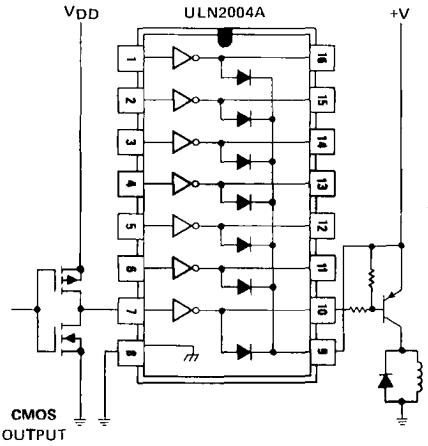
APPLICATION INFORMATION



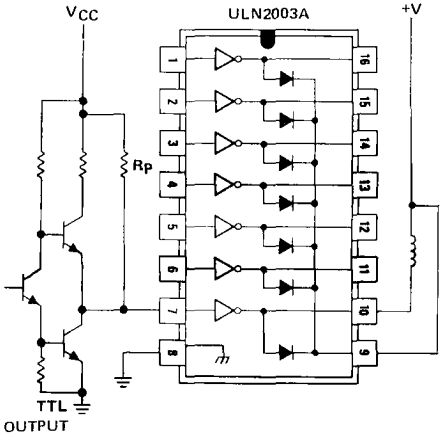
P-MOS TO LOAD



TTL TO LOAD



BUFFER FOR
HIGHER CURRENT LOADS

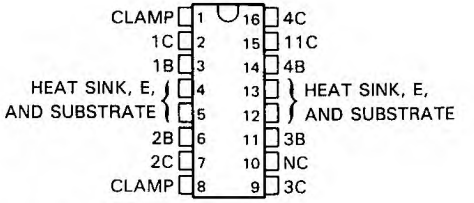


USE OF PULL-UP RESISTORS
TO INCREASE DRIVE CURRENT

D2528, DECEMBER 1979—REVISED SEPTEMBER 1986

- **Output Collector Current . . . 1.5 A Max**
- **2-W Dissipation Rating**
- **High Output-Voltage Capability**
- **Outputs Diode-Clamped for Inductive Loads**
- **Common-Emitter Circuit for Current Sink**
- **ULN2064 and ULN2065 Have TTL Compatible Inputs**
- **ULN2066 and ULN2067 Have CMOS- and PMOS-Compatible Inputs**
- **Designed for Interchangeability With Sprague ULN2064 thru ULN2067, Respectively**

NE PACKAGE
(TOP VIEW)



NC—No internal connection

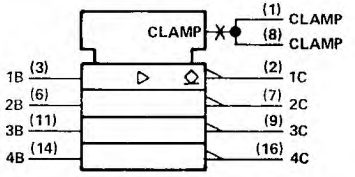
description

The ULN2064, ULN2065, ULN2066, and ULN2067 are monolithic high-voltage, high-current darlington transistor switches. Each comprises four n-p-n darlington pairs. All units feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. Outputs and inputs may each be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. These common-emitter circuits are designed to operate as current sinks to the load.

The ULN2064 and ULN2065 are intended for use with TTL and 5-V MOS logic. The ULN2066 and ULN2067 are intended for use with PMOS and higher-voltage CMOS logic.

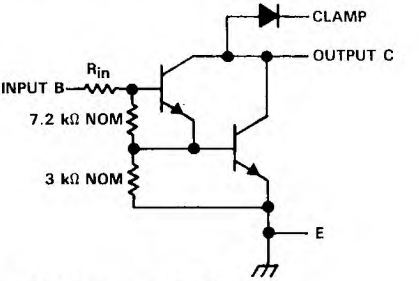
The ULN2064, ULN2065, ULN2066, and ULN2067 are characterized for operation from −20°C to 85°C.

logic symbol†



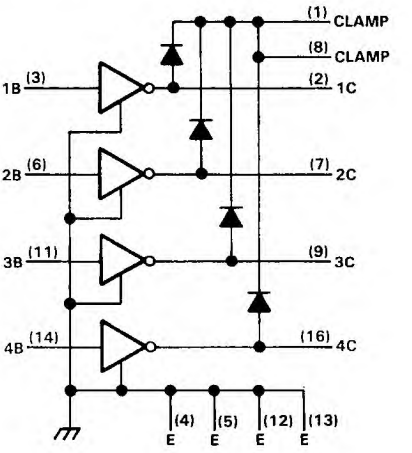
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematic (each darlington pair)



ULN2064, ULN2065: R_{in} = 350 Ω NOM
ULN2066, ULN2067: R_{in} = 3 kΩ NOM

logic diagram



absolute maximum ratings at 25°C free-air temperature for each switch (unless otherwise noted)

	ULN2064	ULN2065	ULN2066	ULN2067	UNIT
Collector-emitter voltage	50	50	50	50	V
Input voltage (see Note 1)	15	15	30	30	V
Peak collector current (see Figures 12, 13, and 14)	1.5	1.5	1.5	1.5	A
Input current	25	25	25	25	mA
Total power dissipation at (or below) 25°C free-air temperature (see Note 2)	2075	2075	2075	2075	mW
Operating free-air temperature range	−20 to 85	−20 to 85	−20 to 85	−20 to 85	°C
Storage temperature range	−55 to 150	−55 to 150	−55 to 150	−55 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds	260	260	260	260	°C

NOTES: 1. All voltage values (unless otherwise noted) are with respect to the emitter/substrate terminal E.
2. For operation above 25°C free-air temperature, derate total power linearly to 1079 mW at 85°C at the rate of 16.6 mW/°C.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	ULN2064 MIN	ULN2064 MAX	ULN2065 MIN	ULN2065 MAX	ULN2066 MIN	ULN2066 MAX	ULN2067 MIN	ULN2067 MAX	UNIT
$V_{CEX(sus)}$	Collector sustaining voltage	1	V_I = 0.4 V, I_C = 100 mA	35		50		35		50		V
I_{CEX}	Collector output cutoff current	2	V_{CE} = 50 V		100				100			μA
			V_{CE} = 50 V, T_A = 70°C		500				500			
			V_{CE} = 80 V				100				100	
			V_{CE} = 80 V, T_A = 70°C				500				500	
$I_{I(on)}$	On-state input current	3	V_I = 2.4 V	1.4	4.3	1.4	4.3					mA
			V_I = 3.75 V	3.3	9.6	3.3	9.6					
			V_I = 5 V					0.6	1.8	0.6	1.8	
			V_I = 12 V					1.7	5.2	1.7	5.2	
$V_{I(on)}$	On-state input voltage	4	V_{CE} = 2 V, I_C = 1 A		2		2		6.5		6.5	V
			V_{CE} = 2 V, I_C = 1.5 A, See Note 3		2.5		2.5		10		10	
$V_{CE(sat)}$	Collector-emitter saturation voltage	5	I_I = 625 μA, I_C = 500 mA		1.1		1.1		1.1		1.1	V
			I_I = 935 μA, I_C = 750 mA		1.2		1.2		1.2		1.2	
			I_I = 1.25 mA, I_C = 1 A		1.3		1.3		1.3		1.3	
			I_I = 2 mA, I_C = 1.25 A, See Note 3		1.4				1.4			
			I_I = 2.25 mA, I_C = 1.5 A, See Note 3				1.5				1.5	
I_R	Clamp-diode reverse current	6	V_R = 50 V		50				50			μA
			V_R = 50 V, T_A = 70°C		100				100			
			V_R = 80 V				50				50	
			V_R = 80 V, T_A = 70°C				100				100	
V_F	Clamp-diode forward voltage	7	I_F = 1 A		1.75		1.75		1.75		1.75	V
			I_F = 1.5 A, See Note 3		2		2		2		2	

NOTE 3: These parameters must be measured on one output at a time using pulse techniques, t_w = 10 ms, duty cycle ≤ 10%.

switching characteristics at 25°C free-air temperature, V_{CC} = 5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 8			1	μs
t_{PHL}	Propagation delay time, high-to-low-level output				1.5	μs

PARAMETER MEASUREMENT INFORMATION

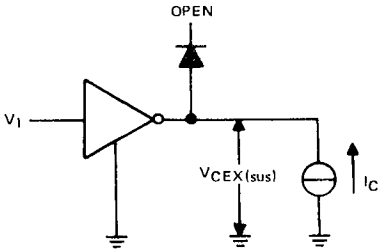


FIGURE 1. $V_{CEX(sus)}$

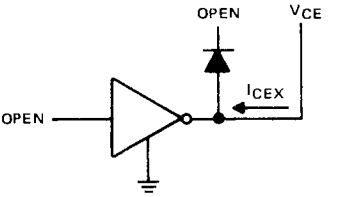


FIGURE 2. I_{CEX}

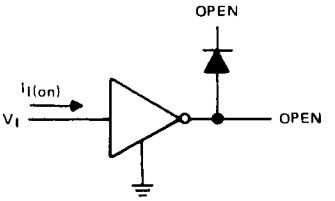


FIGURE 3. $I_{I(on)}$

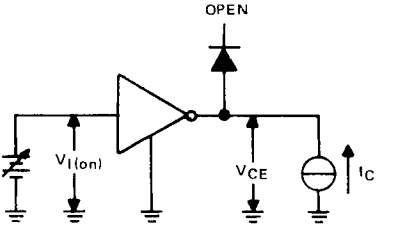


FIGURE 4. $V_{I(on)}$

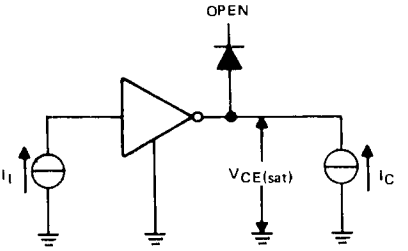


FIGURE 5. $V_{CE(sat)}$

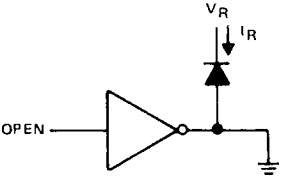


FIGURE 6. I_R

PARAMETER MEASUREMENT INFORMATION

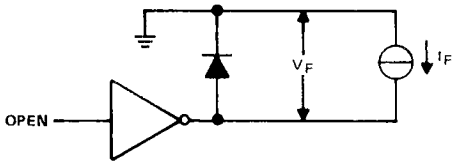
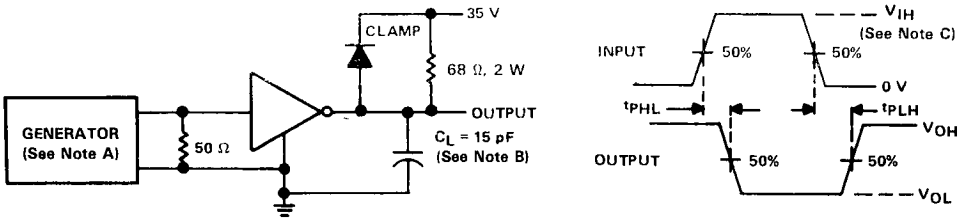


FIGURE 7. V_F



NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 50 kHz, duty cycle = 10%, Z_o = 50 Ω.
B. C_L includes all probe and stray capacitance.
C. V_{IH} = 2.5 V for ULN2064 and ULN2065. V_{IH} = 10 V for ULN2065 and ULN2067.

FIGURE 8. SWITCHING TIMES

ELECTRICAL CHARACTERISTICS

COLLECTOR CURRENT
VS
BASE CURRENT

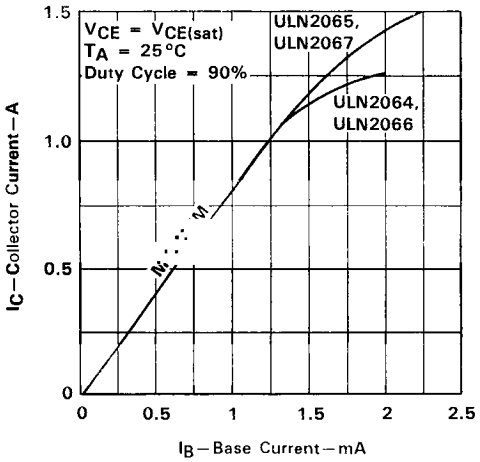


FIGURE 9

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

THERMAL INFORMATION

MAXIMUM COLLECTOR CURRENT
vs
DUTY CYCLE

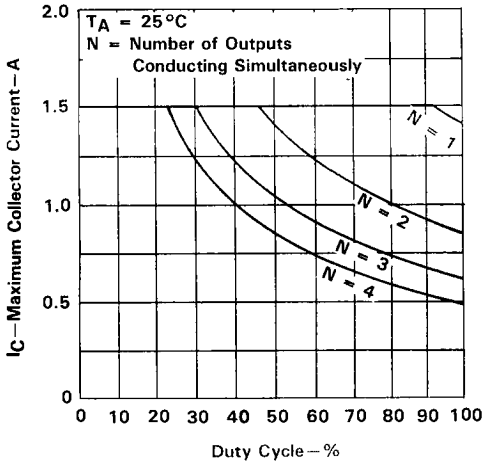


FIGURE 10

MAXIMUM COLLECTOR CURRENT
vs
DUTY CYCLE

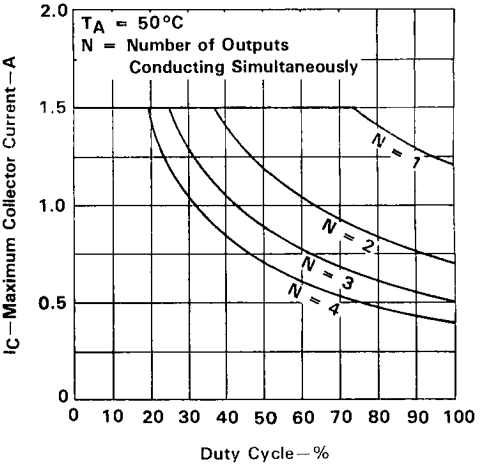


FIGURE 11

MAXIMUM COLLECTOR CURRENT
vs
DUTY CYCLE

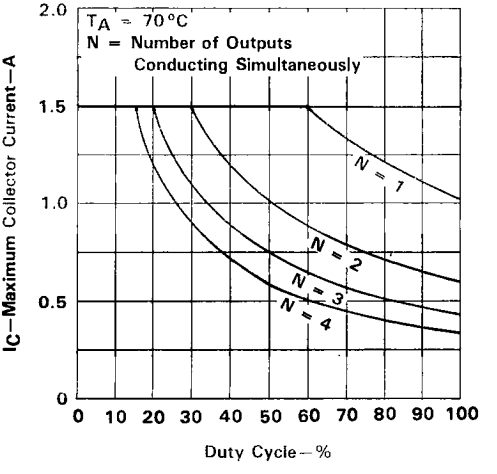


FIGURE 12

APPLICATION INFORMATION

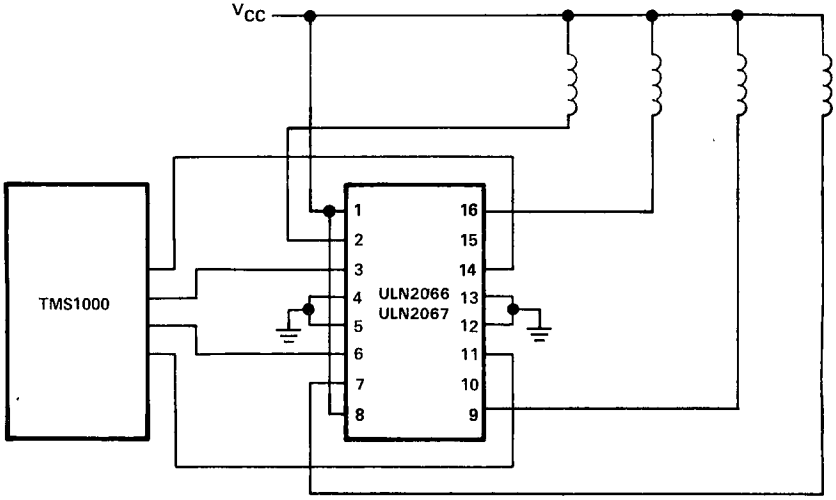


FIGURE 13. RELAY DRIVER INTERFACE

TEXAS INSTRUMENTS
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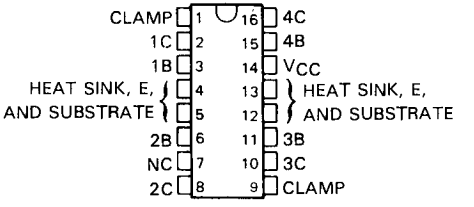
D2579, MAY 1980—REVISED SEPTEMBER 1986

- Output Collector Current . . . 1.5 A Max
- 2-W Dissipation Rating
- High Output-Voltage Capability
- Preamp for High Current Gain
- Outputs Diode-Clamped for Inductive Loads
- Common-Emitter Circuit for Current Sink
- Inputs Compatible With TTL and 5-V CMOS
- Designed for Interchangeability With Sprague ULN2068 and ULN2069

NE PACKAGE
(TOP VIEW)



NC—No internal connection

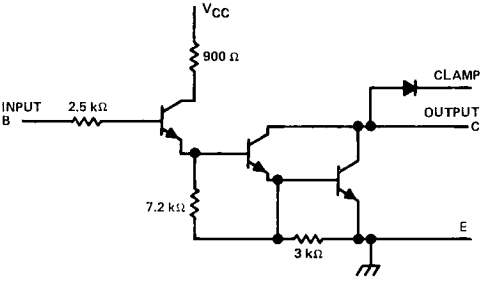
description

The ULN2068 and ULN2069 are monolithic integrated circuits each consisting of four high-voltage, high-current n-p-n cascaded transistor switches. Each switch includes a first stage compatible with both TTL and 5-V CMOS signal levels. The second and third stages form uncommitted-collector outputs with common-cathode clamp diodes for switching inductive loads.

The ULN2068 and ULN2069 can sink up to 1.5 A per switch. Applications include logic buffers, MOS drivers, memory drivers, line drivers, relay drivers, hammer drivers, lamp drivers, and display drivers (LED and gas discharge).

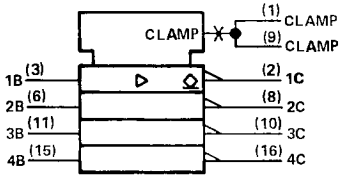
The ULN2068 and ULN2069 are characterized for operation from −20°C to 85°C.

schematic (each switch)



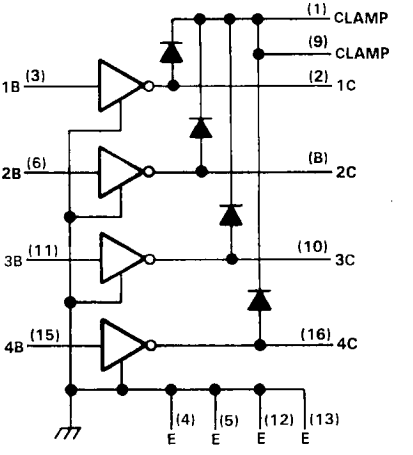
Resistor values shown are nominal.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings at 25°C free-air temperature for each switch (unless otherwise noted)

	[illegible]	[illegible]	[illegible]
Collector-emitter voltage	50	50	V
Supply voltage, V_{CC} (see Note 1)	10	10	V
Input voltage	15	15	V
Peak collector current (see Figures 10, 11, and 12)	1.5	1.5	A
Total power dissipation at (or below) 25°C free-air temperature (see Note 2)	2075	2075	mW
Operating free-air temperature range	−20 to 85	−20 to 85	°C
Storage temperature range	−55 to 150	−55 to [illegible]	°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds	260	260	°C

NOTES: 1. All voltage values (unless otherwise noted) are with respect to the emitter/substrate terminal E.
2. For operation above 25°C free-air temperature, derate total power linearly to 1079 mW at 85°C at the rate of 16.6 mW/°C.

electrical characteristics at 25°C free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	ULN2068		ULN2069		UNIT
				MIN	MAX	MIN	MAX	
$V_{CEX(sus)}$	Collector sustaining voltage	1	V_I = 0.4 V, I_C = 100 mA	35		50		V
I_{CEX}	Collector output cutoff current	2	V_{CE} = 50 V		100			μA
			V_{CE} = 50 V, T_A = 70°C		500			
			V_{CE} = 80 V				100	
			V_{CE} = 80 V, T_A = 70°C					
$I_{I(on)}$	On-state input current	3	V_I = 2.4 V					μA
			V_I = 3.75 V					
$V_{I(on)}$	On-state input voltage	4	V_{CE} = 2 V, I_C = 1.5 A, See Note 3		2.4		2.4	V
$V_{CE(sat)}$	Collector-emitter saturation voltage	5	V_I = 2.4 V, I_C = 500 mA		1.1		1.1	V
			V_I = 2.4 V, I_C = 750 mA		1.2		1.2	
			V_I = 2.4 V, I_C = 1 A		1.3		1.3	
			V_I = 2.4 V, I_C = 1.25 A, See Note 3		1.4			
			V_I = 2.4 V, I_C = 1.5 A, See Note 3				1.5	
I_R	Clamp-diode reverse current	6	V_R = 50 V		50			μA
			V_R = 50 V, T_A = 70°C		100			
			V_R = 80 V				50	
			V_R = 80 V, T_A = 70°C				100	
V_F	Clamp-diode forward voltage	7	I_F = 1 A		1.75		1.75	V
			I_F = 1.5 V, See Note 3		2		2	
I_{CC}	Supply current (only one switch conducting)	8	V_I = 2.4 V, I_C = 500 mA		6		6	mA

NOTE 3: These parameters must be measured on one output at a time using pulse techniques, t_w = 10 ms, duty cycle ≤ 10%.

switching characteristics at 25°C free-air temperature, V_{CC} = 5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 9			1	μs
t_{PHL}	Propagation delay time, high-to-low-level output				1.5	μs

TEXAS INSTRUMENTS
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PARAMETER MEASUREMENT INFORMATION

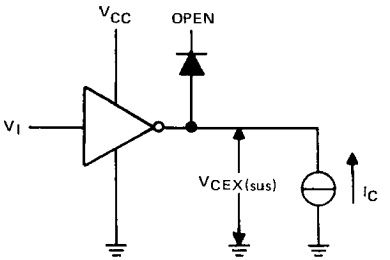


FIGURE 1. $V_{CEX(sus)}$

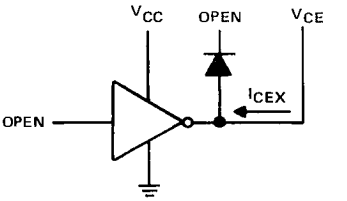


FIGURE 2. I_{CEX}

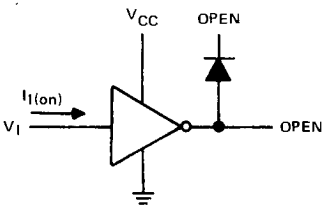


FIGURE 3. $I_{I(on)}$

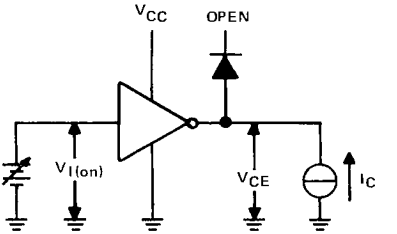


FIGURE 4. $V_{I(on)}$

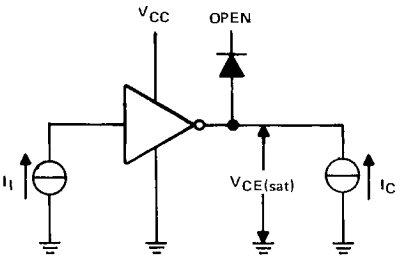


FIGURE 5. $V_{CE(sat)}$

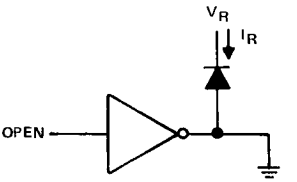


FIGURE 6. I_R

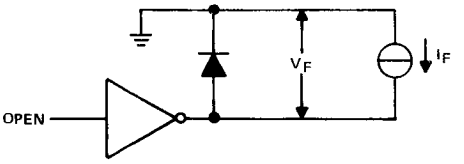


FIGURE 7. V_F

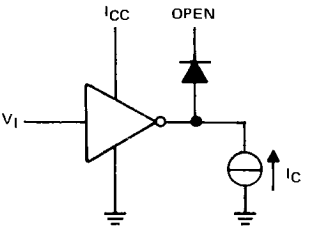
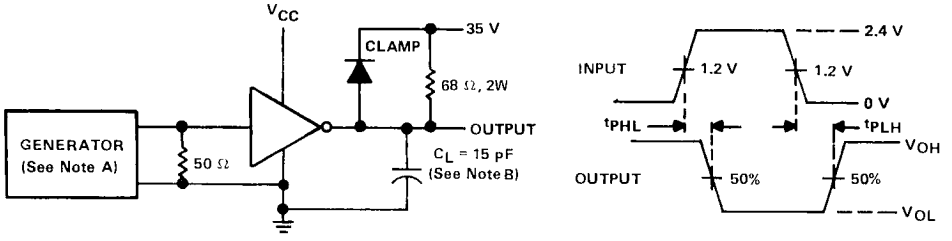


FIGURE 8. I_{CC}

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 50 kHz, duty cycle = 10%, Z_o = 50 Ω.
B. C_L includes all probe and stray capacitance.

FIGURE 9. SWITCHING TIMES

THERMAL INFORMATION

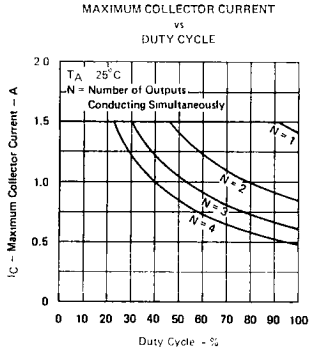


FIGURE 10

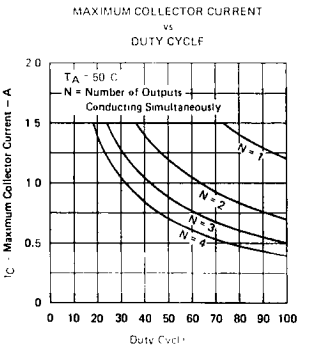


FIGURE 11

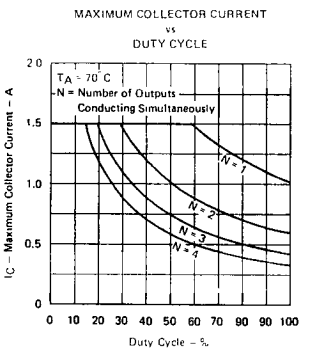


FIGURE 12

APPLICATION INFORMATION

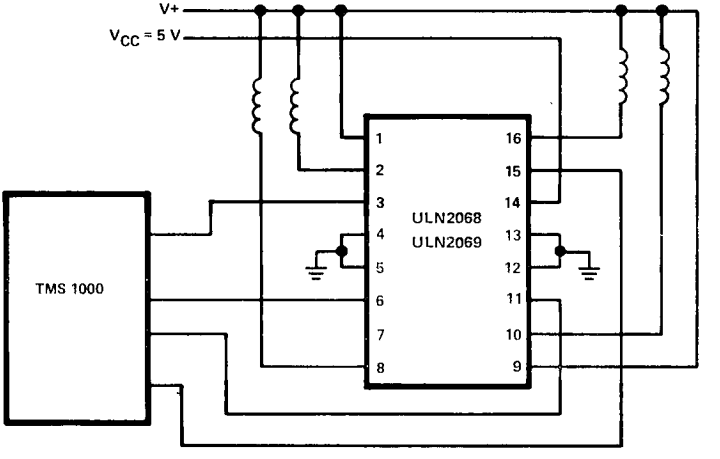
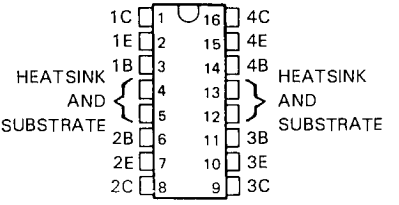


FIGURE 13. RELAY DRIVER INTERFACE

D2580, MAY 1980—REVISED SEPTEMBER 1986

- Output Collector Current . . . 1.5 A Max
- 2-W Dissipation Rating
- High Output-Voltage Capability
- Output Sink- or Source-Current Capabilities
- Input Compatible with TTL or 5-V CMOS
- Designed for Interchangeability with Sprague ULN2074 and ULN2075

NE PACKAGE
(TOP VIEW)



description

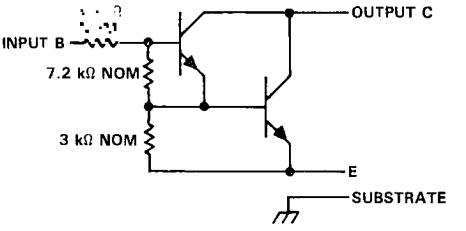
The ULN2074 and ULN2075 are monolithic, quadruple, high-voltage, high-current n-p-n darlington-transistor amplifier devices. They feature high-voltage outputs with collector-current ratings of 1.5 A for each Darlington pair.

The ULN2074 and ULN2075 are unique general-purpose devices, each featuring uncommitted collectors and emitters to allow for either sinking or sourcing the output current. These devices offer the system designer the flexibility of tailoring the circuit to the application. Typical applications include logic buffers, relay drivers, lamp drivers, and hammer drivers.

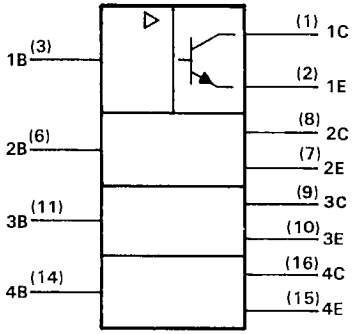
For proper operation, the substrate must be connected to the most negative voltage.

The ULN2074 and ULN2075 are characterized for operation from −20°C to 85°C.

schematic (each switch)



logic symbol†



‡ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings at 25°C free-air temperature for each switch (unless otherwise noted)

	ULN2074	ULN2075	UNIT
Collector-emitter voltage	50	80	V
Input voltage with respect to substrate	30	60	V
Peak collector current (see Figures 9, 10, and 11)	1.5	1.5	A
Input current	25	25	mA
Total power dissipation at (or below) 25°C free-air temperature (see Note 1)	2075	2075	mW
Operating free-air temperature range	−20 to 85	−20 to 85	°C
Storage temperature range	−55 to	−55 to	°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds	260	260	°C

NOTE 1: For operation above 25°C free-air temperature, derate total power linearly to 1079 mW at 85°C at the rate of 16.6 mW/°C.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS	ULN2074		ULN2075		UNIT
				MIN	MAX	MIN	MAX	
$V_{CEX(sus)}$	Collector sustaining voltage	1	V_I = 0.4 V, I_C = 100 mA	35		50		V
I_{CEX}	Collector output cutoff current	2	V_{CE} = 50 V					μA
			V_{CE} = 50 V, T_A = 70°C					
			V_{CE} = 80 V				100	
			V_{CE} = 80 V, T_A = 70°C				500	
$I_{I(on)}$	On-state input current	3	V_I = 2.4 V	2	4.3	2	4.3	mA
			V_I = 3.75 V	4.5	9.6	4.5	9.6	
$V_{I(on)}$	On-state input voltage	4	V_{CE} = 2 V, I_C = 1 A		2		2	V
			V_{CE} = 2 V, I_C = 1.5 A, See Note 2		2.5		2.5	
$V_{CE(sat)}$	Collector-emitter saturation voltage	5	I_I = [illegible] μA, I_C = 500 mA		1.1		1.1	V
			I_I = 935 μA, I_C = 750 mA		1.2		1.2	
			I_I = 1.25 mA, I_C = 1 A		1.3		1.3	
			I_I = 2 mA, I_C = 1.25 A, See Note 2		1.4			
			I_I = 2.25 mA, I_C = 1.5 A, See Note 2				1.5	

NOTE 2: These parameters must be measured on one output at a time using pulse techniques, t_w = 10 ms, duty cycle ≤ 10%.

switching characteristics at 25°C free-air temperature, V_{CC} = 5 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 6			1	μs
t_{PHL}	Propagation delay time, high-to-low-level output				1.5	μs

PARAMETER MEASUREMENT INFORMATION

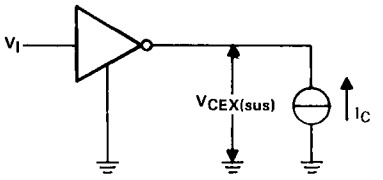


FIGURE 1. $V_{CEX(sus)}$

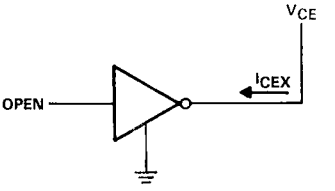


FIGURE 2. I_{CEX}

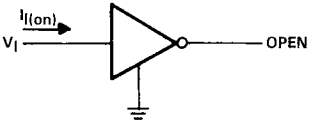


FIGURE 3. $I_{I(on)}$

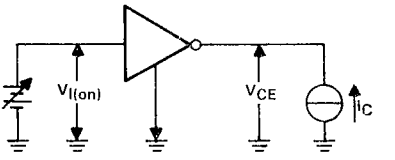


FIGURE 4. $V_{I(on)}$

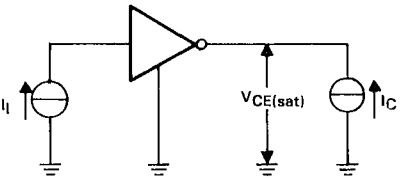
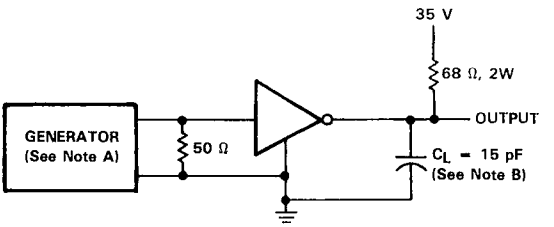
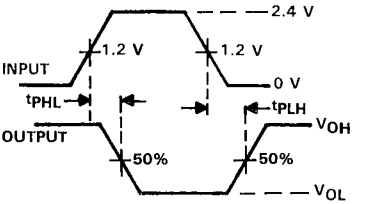


FIGURE 5. $V_{CE(sat)}$



TEST CIRCUITS



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 50 kHz, duty cycle = 10%, Z_o = 50 Ω.
B. C_L includes all probe and stray capacitance.

FIGURE 6. SWITCHING CHARACTERISTICS

ELECTRICAL CHARACTERISTICS

INPUT CURRENT
vs
INPUT VOLTAGE

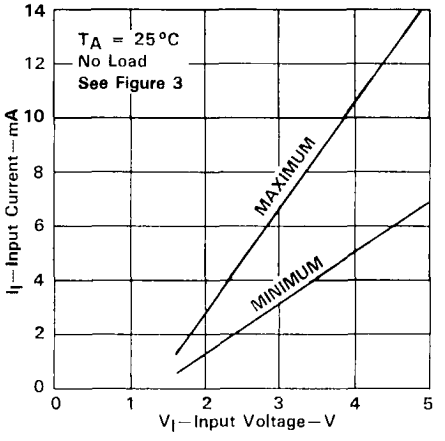


FIGURE 7

COLLECTOR CURRENT
vs
BASE CURRENT

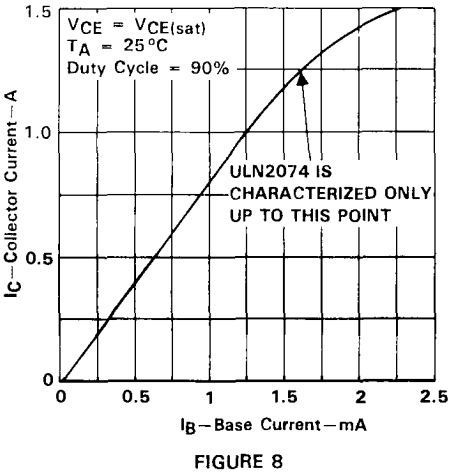


FIGURE 8

THERMAL INFORMATION

MAXIMUM COLLECTOR CURRENT
vs
DUTY CYCLE

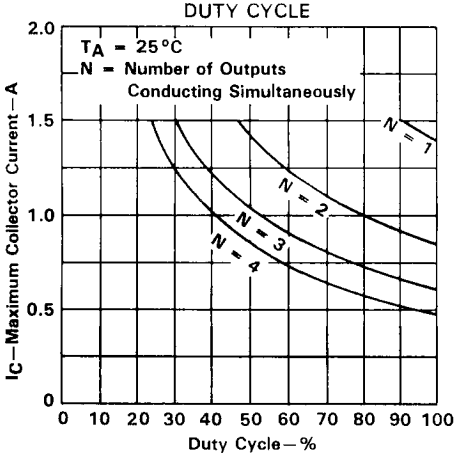


FIGURE 9

MAXIMUM COLLECTOR CURRENT
vs
DUTY CYCLE

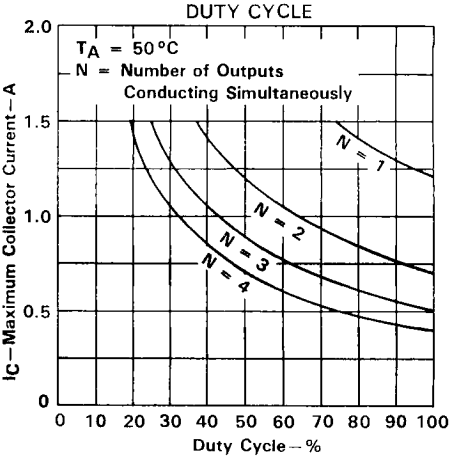


FIGURE 10

MAXIMUM COLLECTOR CURRENT
vs
DUTY CYCLE

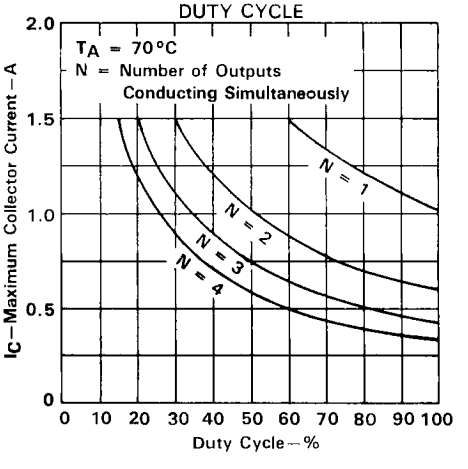


FIGURE 11

APPLICATION INFORMATION

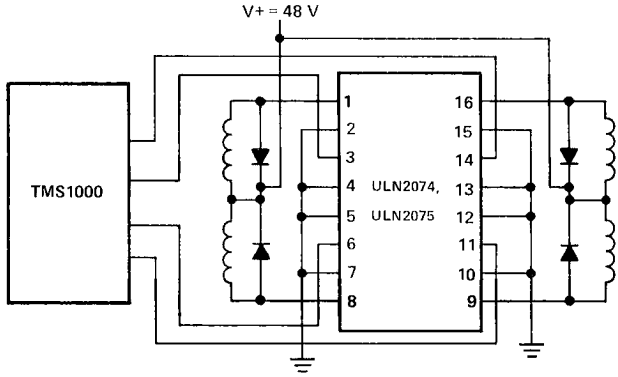


FIGURE 12. RELAY DRIVER INTERFACE WITH EXTERNAL CLAMP DIODES